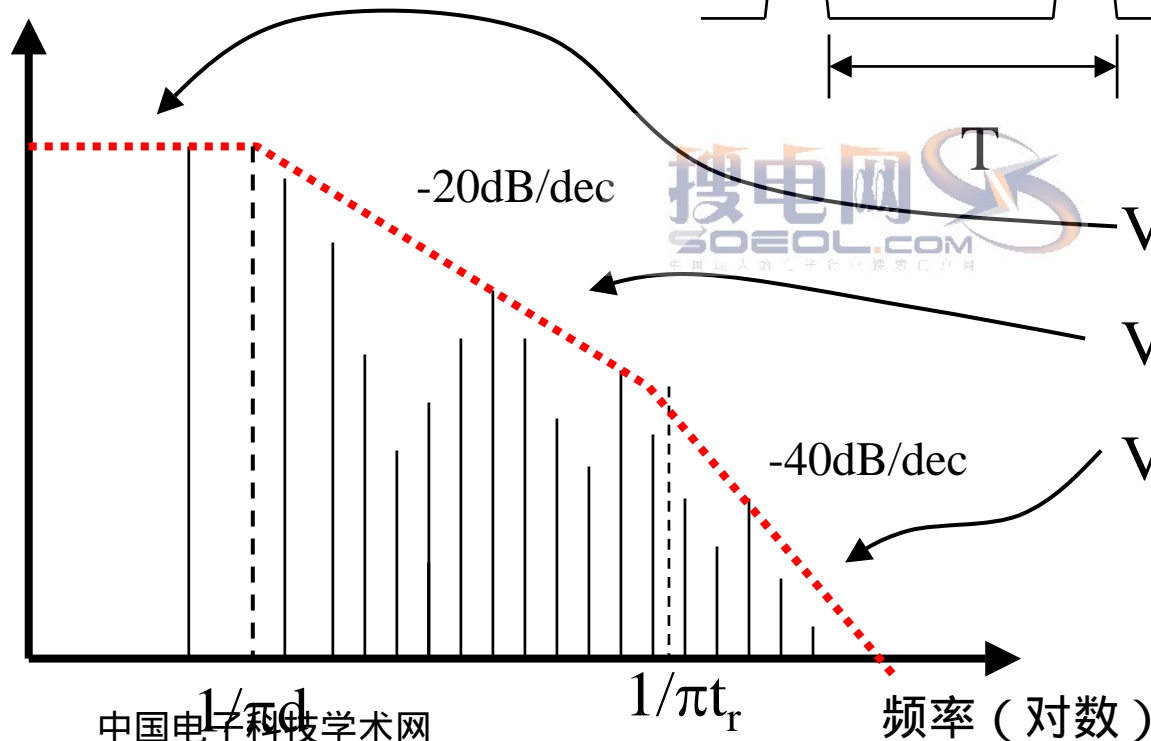
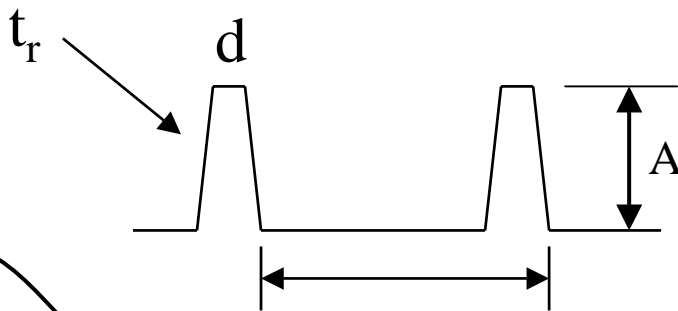


# PCB的电磁兼容设计



# 脉冲信号的频谱

谐波幅度  
(电压或电流)

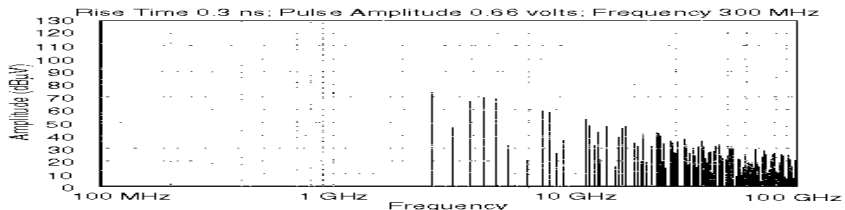
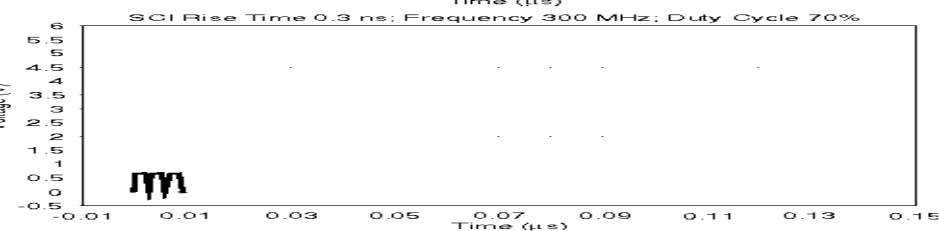
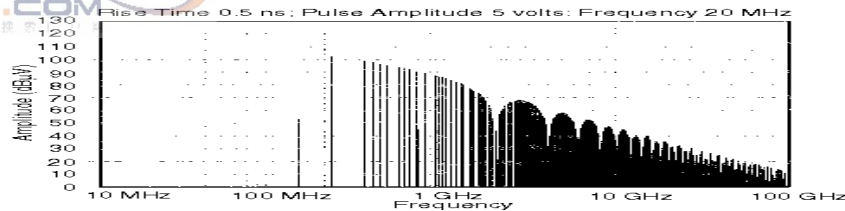
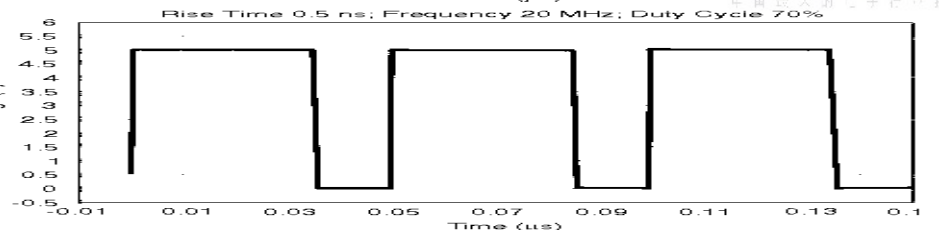
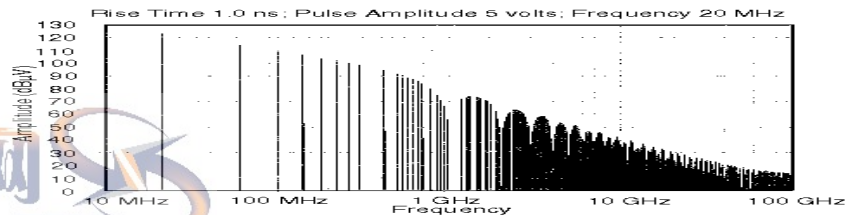
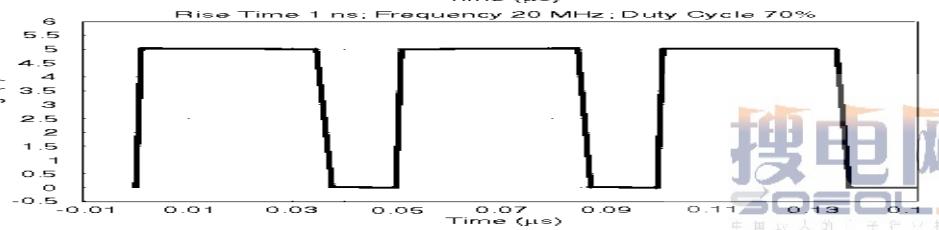
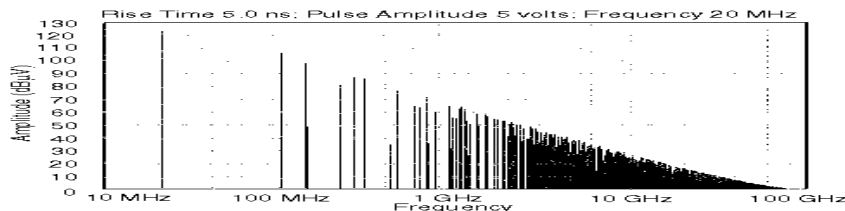
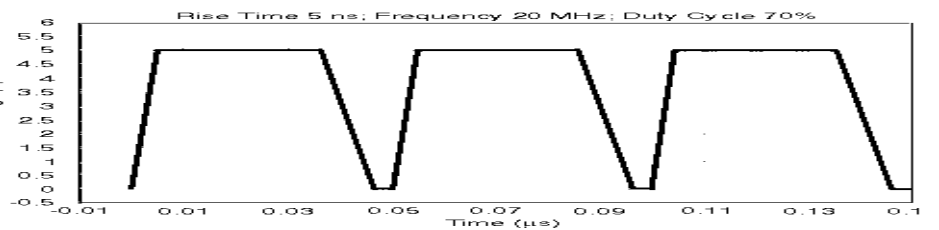


$$V(\text{ or } I) = 2A(d+t_r)/T$$

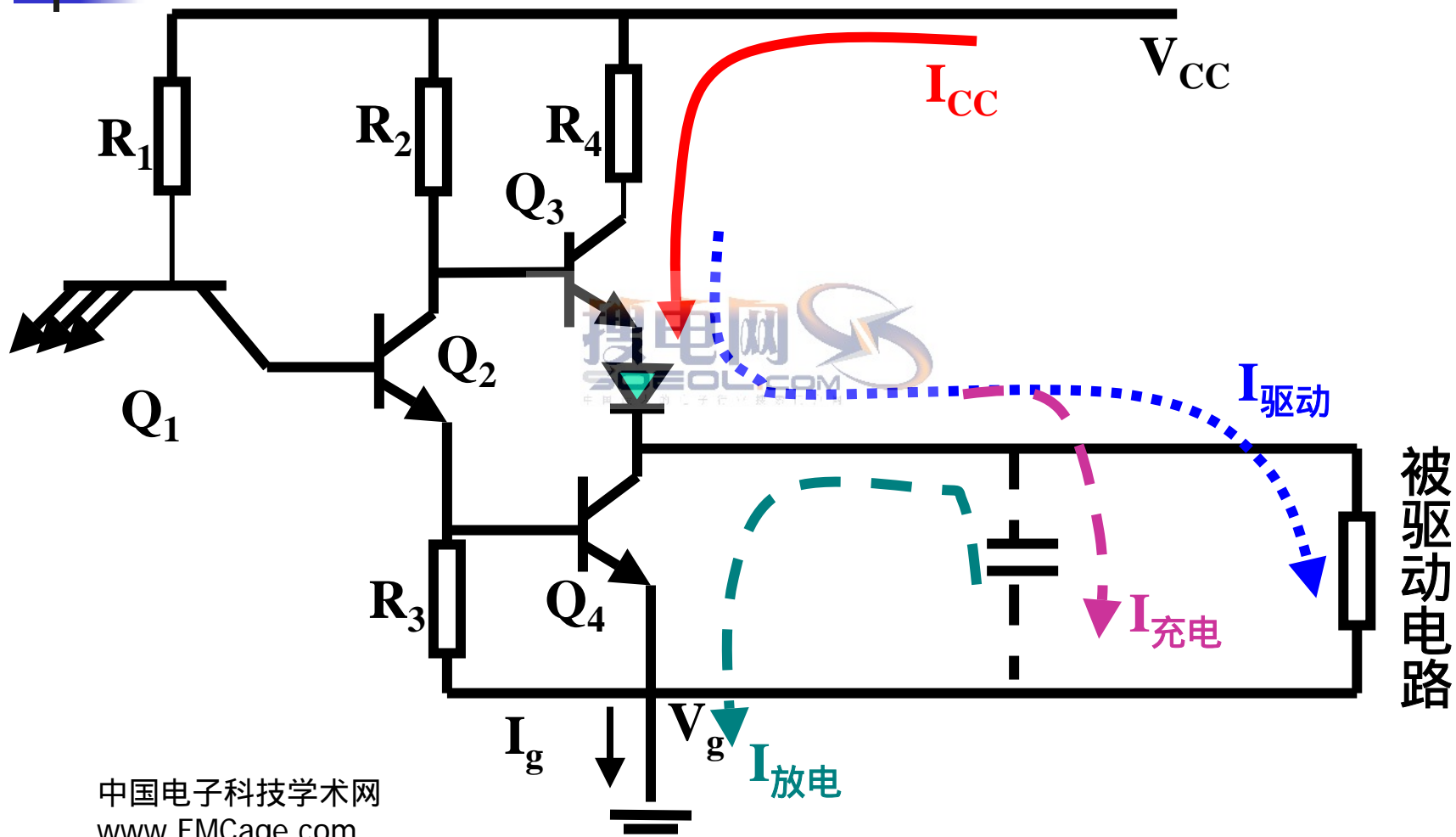
$$V(\text{ or } I) = 0.64A/Tf$$

$$V(\text{ or } I) = 0.2A/Tt_r f^2$$

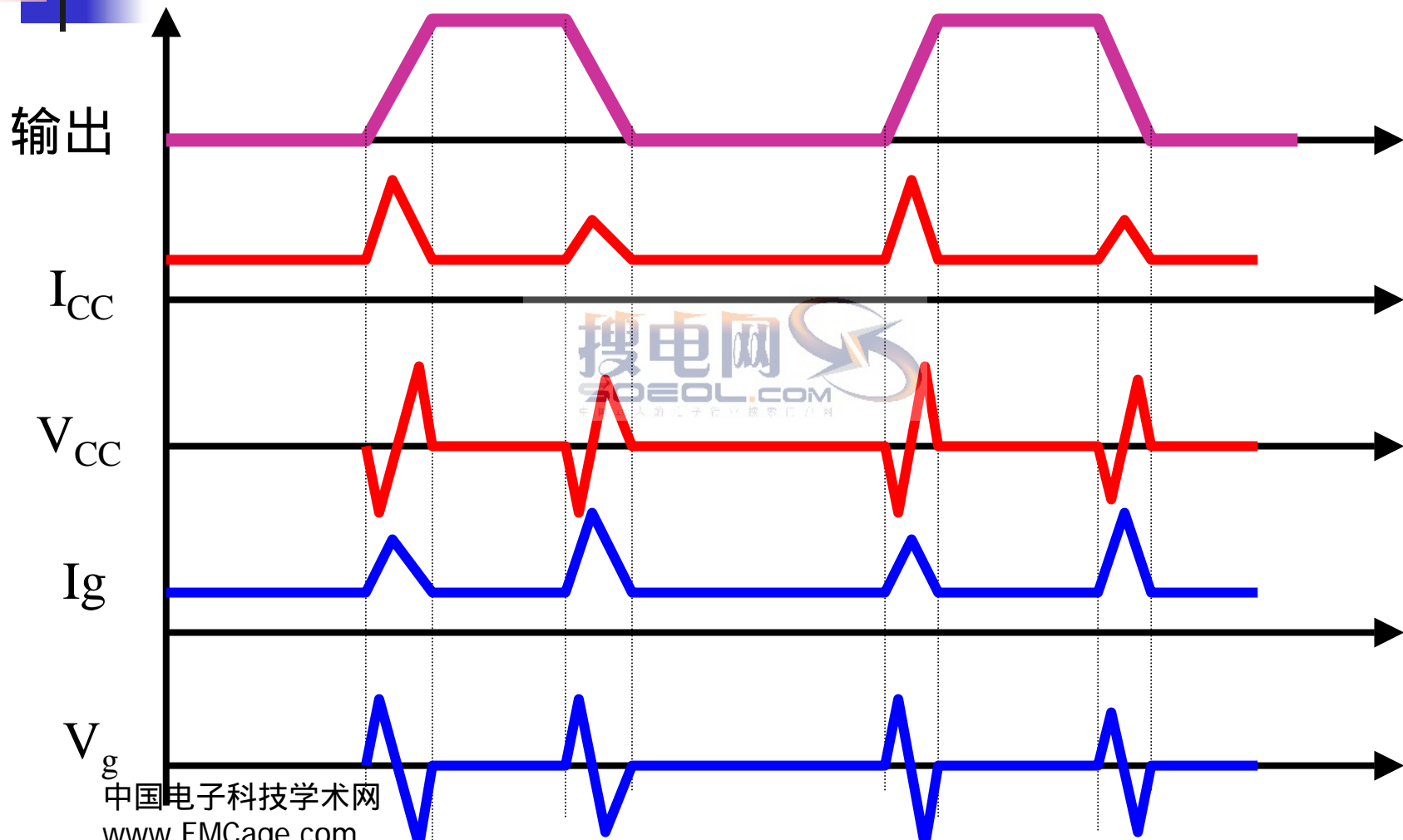
# 上升沿越陡高频越丰富



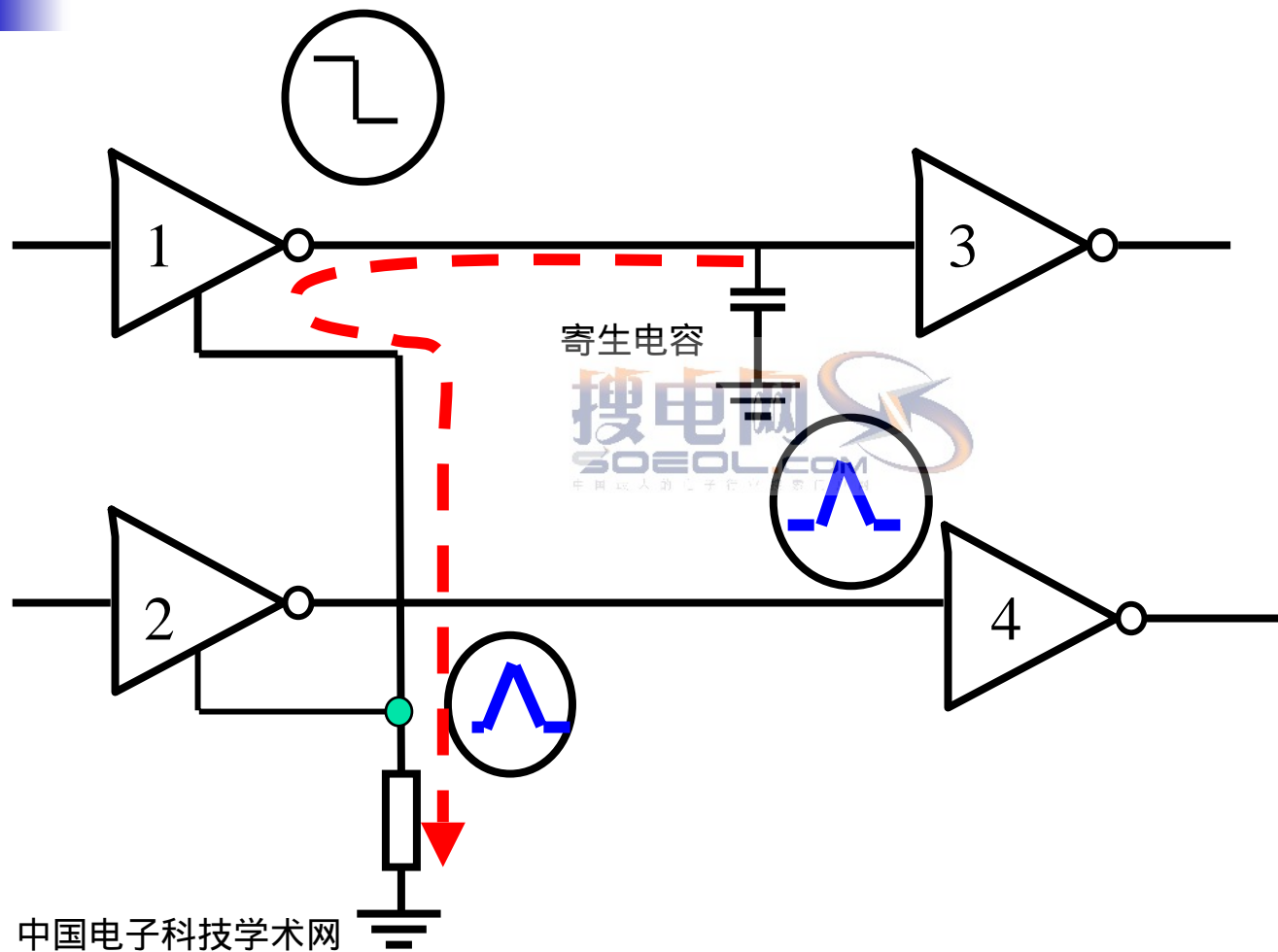
# 地线和电源线上的噪声



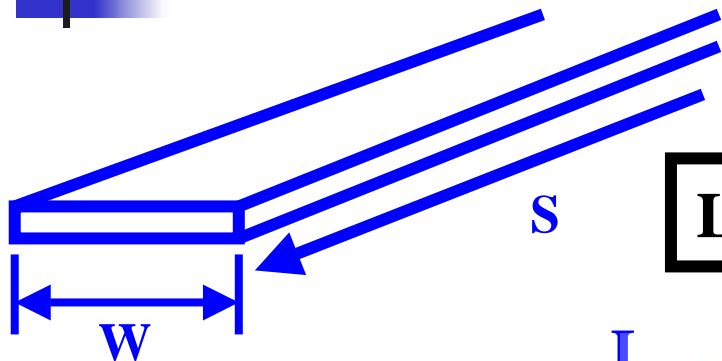
# 电源线、地线噪声电压波形



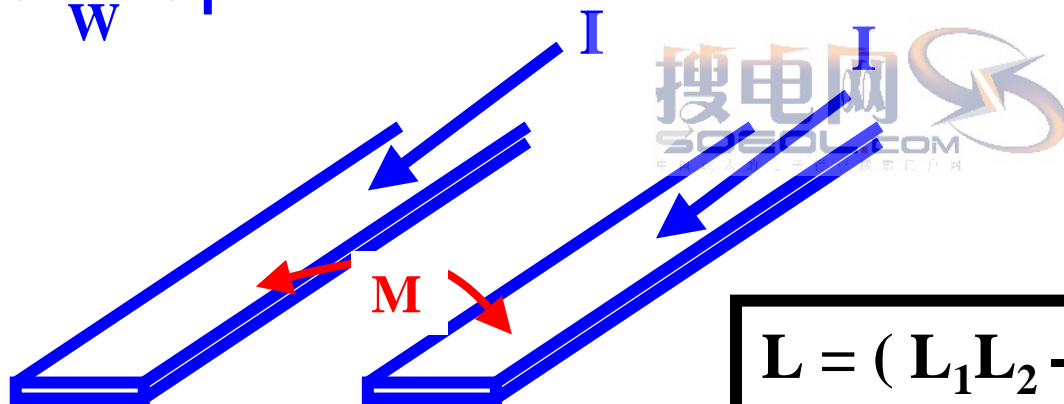
# 地线干扰对电路的影响



# 线路板走线的电感



$$L = 0.002S(2.3 \lg(2S/W) + 0.5) \mu\text{H}$$

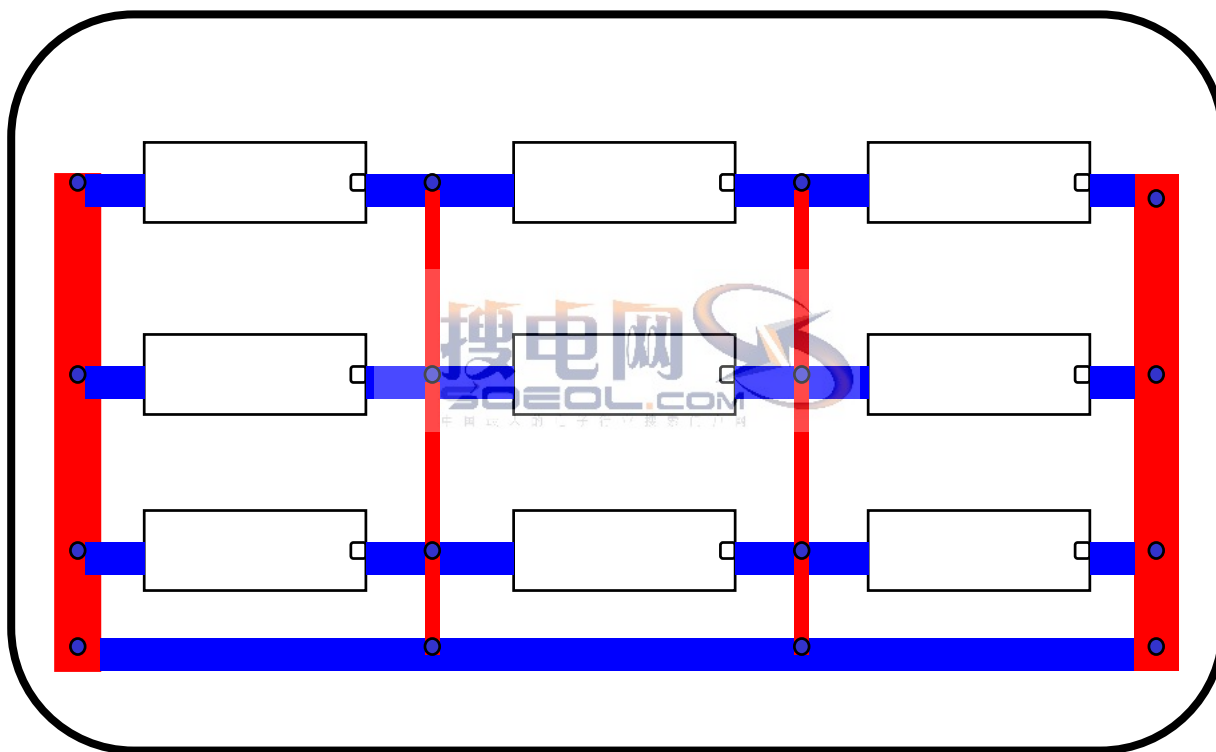


$$L = (L_1 L_2 - M^2) / (L_1 + L_2 - 2M)$$

若： $L_1 = L_2$

$$L = (L_1 + M) / 2$$

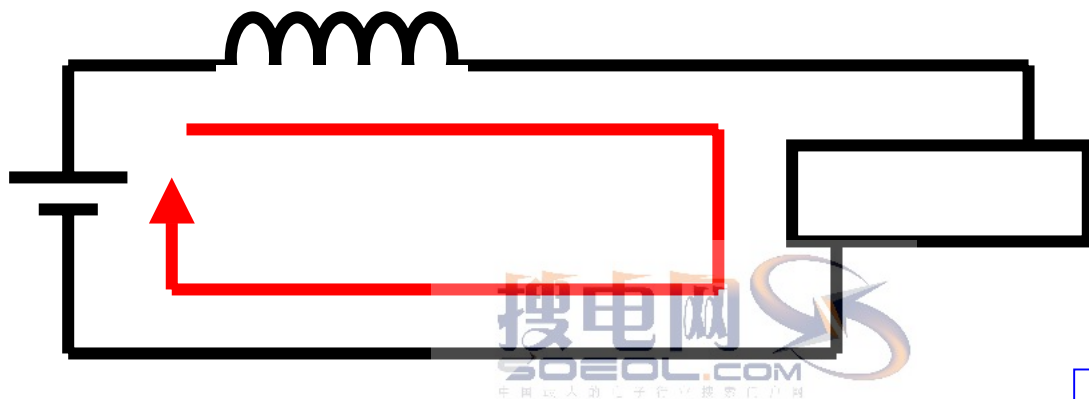
# 地线网格



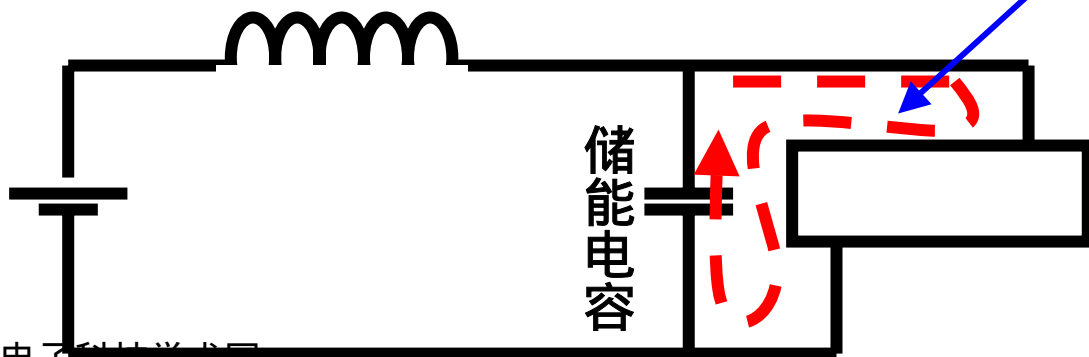


# 电源线噪声的消除

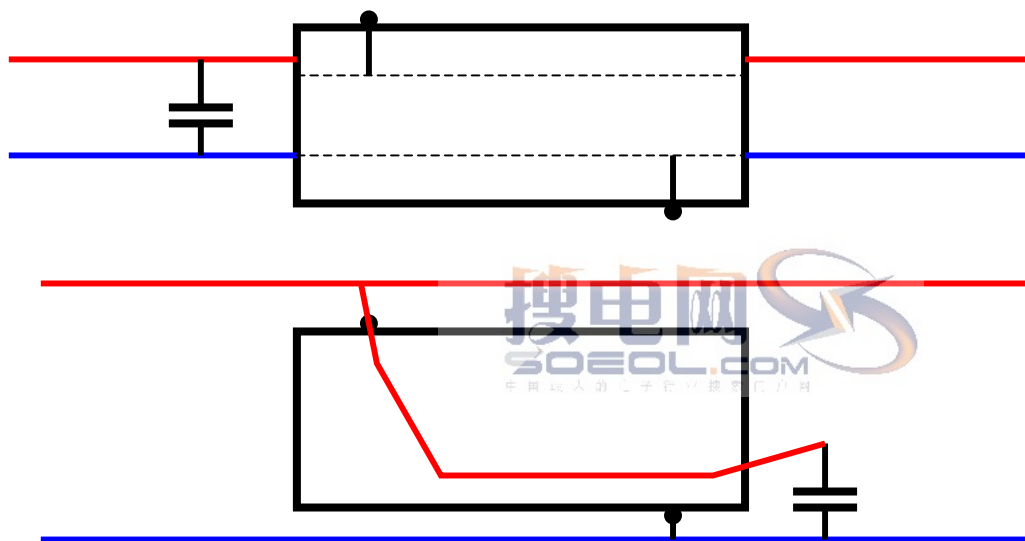
电源线电感



这个环路尽量小



# 电源解耦电容的正确布置



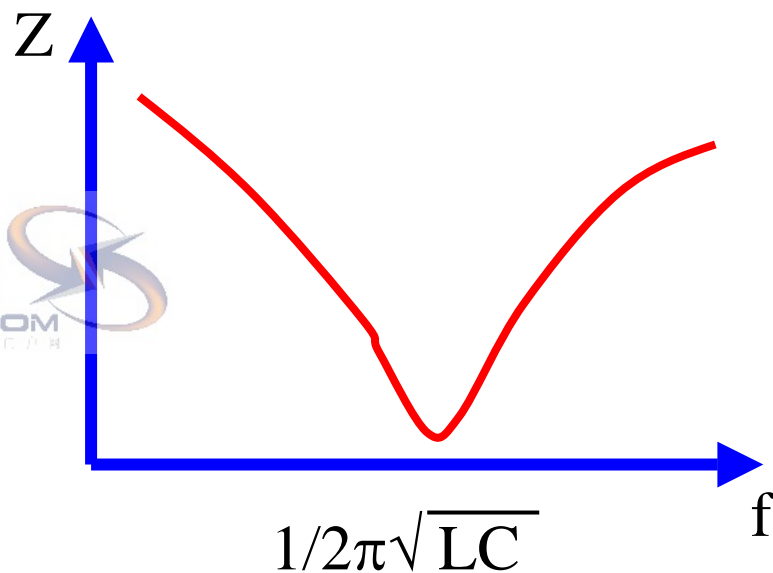
尽量使电源线与地线靠近

# 解耦电容的选择

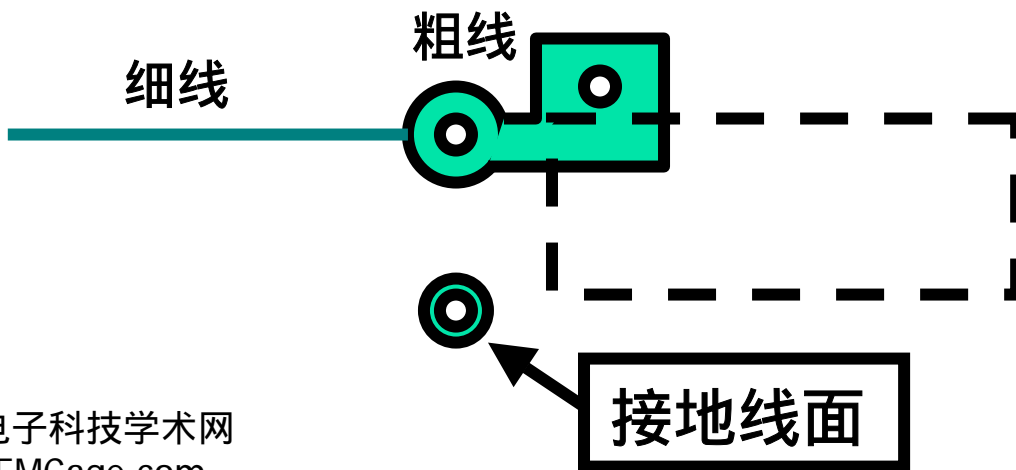
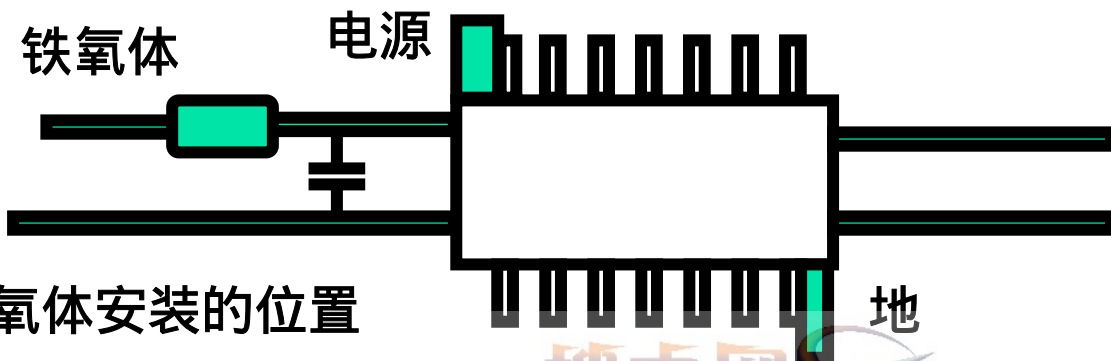
$$C = \frac{dI \, dt}{dV}$$

各参数含义：

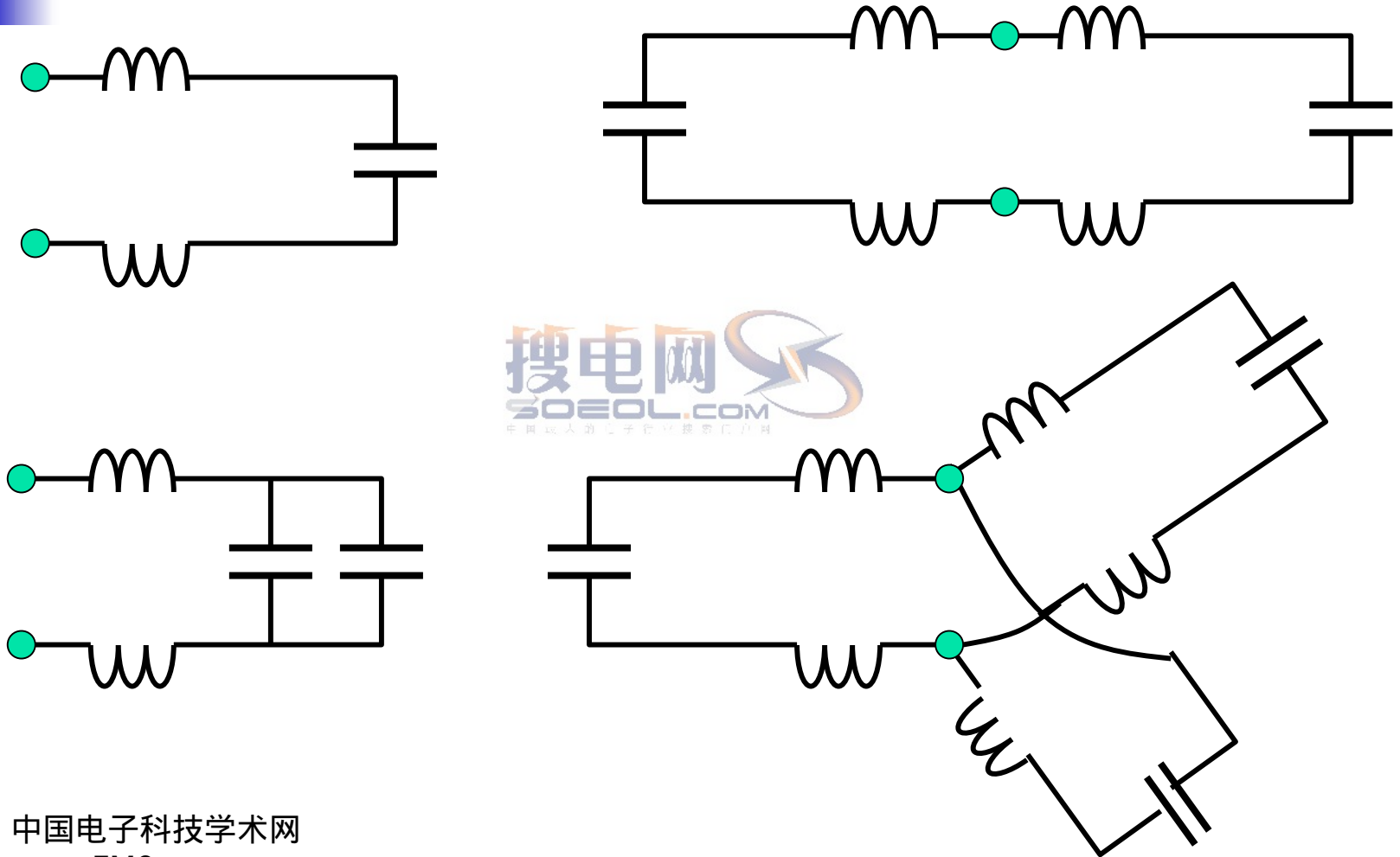
在时间 $dt$ 内，电源线上出现了瞬间电流 $dI$ ， $dI$ 导致了电源线上出现电压跌落 $dV$ 。



# 增强解耦效果的方法

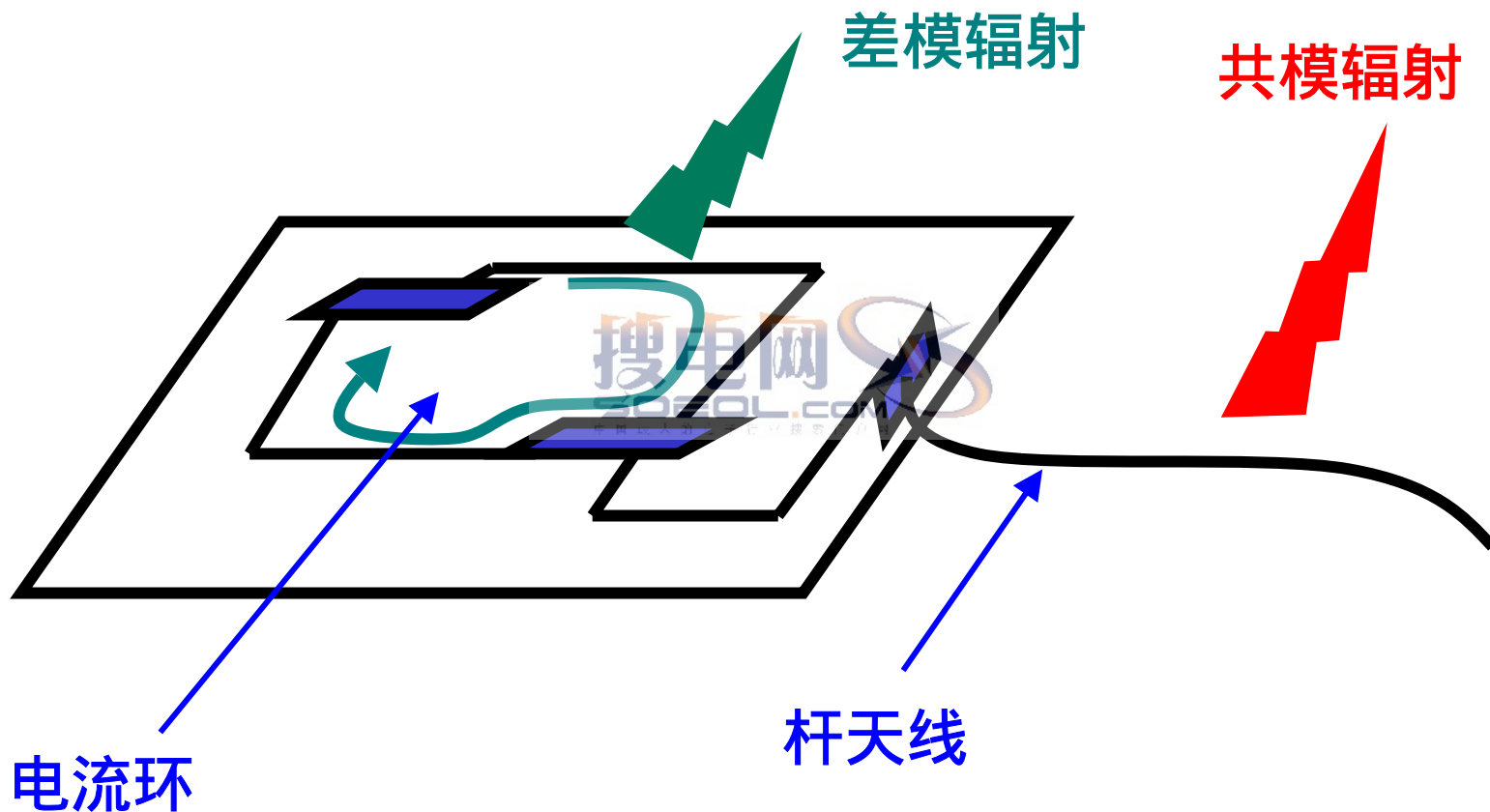


# 多个电容并联加强解耦效果



搜电网  
SOEOL.COM  
中国最大的电子元器件搜索引擎

# 线路板的两种辐射机理

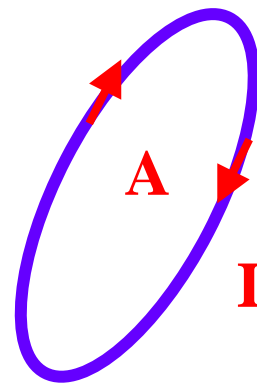


# 电流环路产生的辐射

近场区内:  $H = IA / (4\pi D^3)$       A/m

$E = Z_0 IA / (2\lambda D^2)$       V/m

$Z_W = Z_0 (2\pi D / \lambda)$

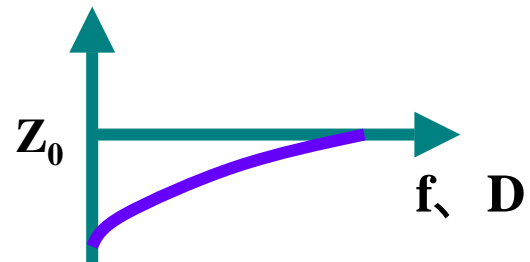


远场区内:  $H = \pi IA / (\lambda^2 D)$       A/m

$E = Z_0 \pi IA / (\lambda^2 D)$       V/m

$Z_W = Z_0 = 377$        $\Omega$

随频率、距离增加而增加

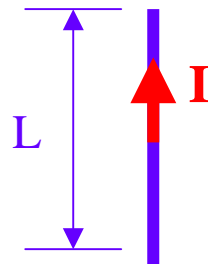


# 导线的辐射

近场区内:  $H = I L / (4\pi D^2)$       A/m

$E = Z_0 I L \lambda / (8 \pi^2 D^3)$       V/m

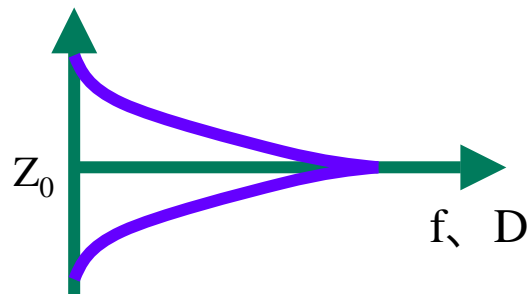
$Z_w = Z_0 (\lambda / 2\pi D)$        $\Omega$



远场区内:  $H = I L / (2\lambda D)$       A/m

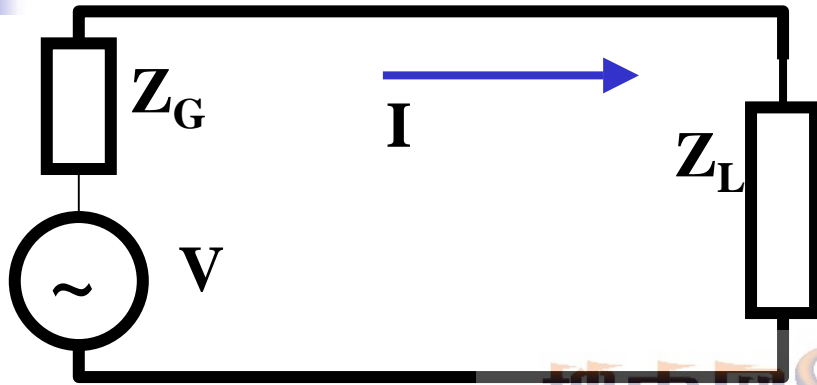
$E = Z_0 I L / (2\lambda D)$       V/m

随频率、距离增加而减小





# 实际电路的辐射



$$Z_C = Z_G + Z_L$$

环路面积 = A

近场： $Z_C \geq 7.9 D f$       $E = 7.96 V A / D^3$      ( $\mu V/m$ )

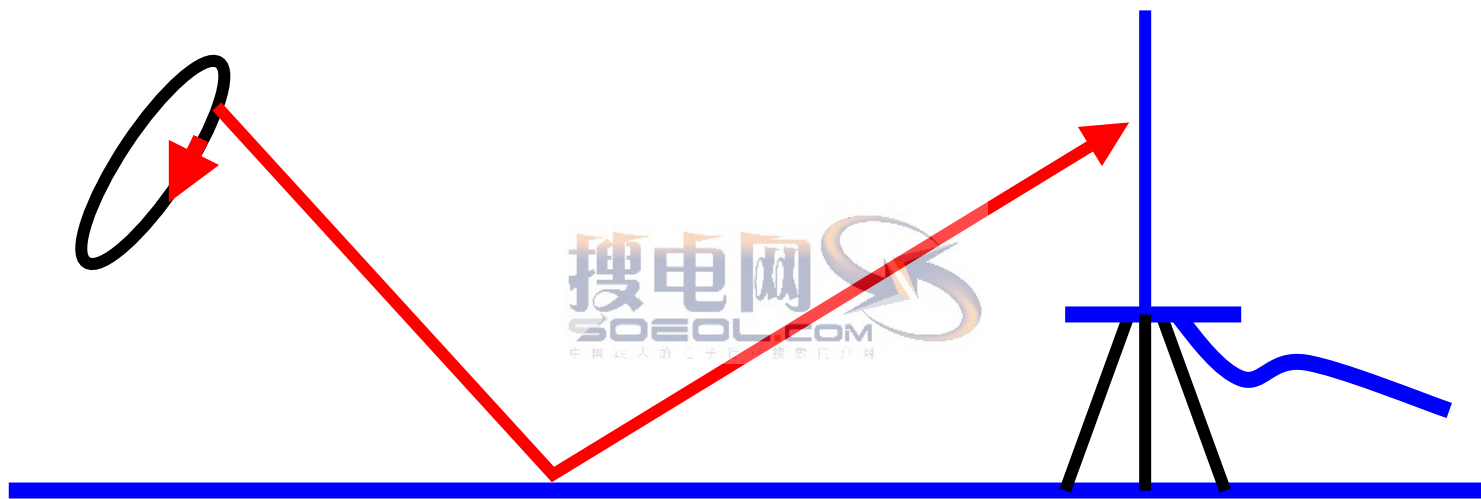
$Z_C \leq 7.9 D f$  ,  $E = 63 I A f / D^2$      ( $\mu V/m$ )

$H = 7.96 I A / D^3$      ( $\mu A/m$ )

远场：

$E = 1.3 I A f^2 / D$      ( $\mu V/m$ )

# 常用的差模辐射预测公式

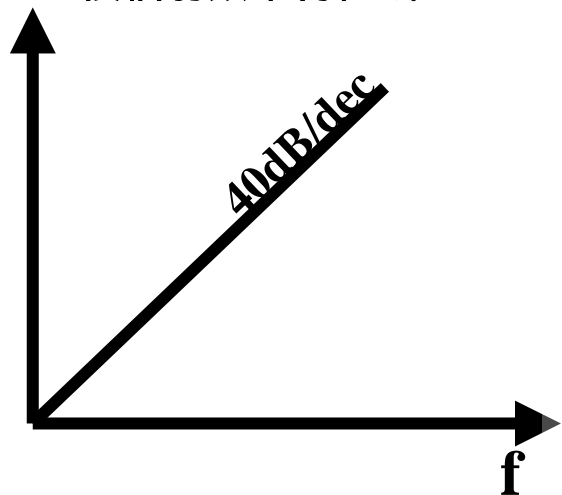


考虑地面反射时：

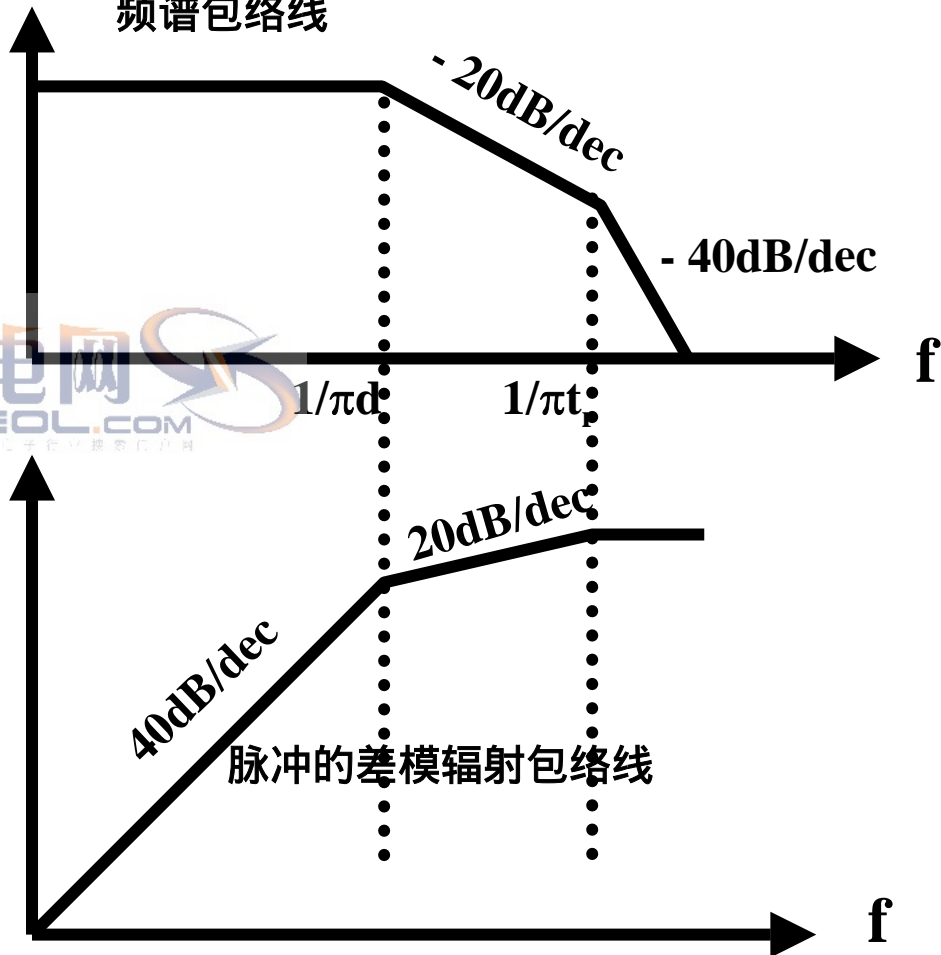
$$E = 2.6 I A f^2 / D \quad (\mu V/m)$$

# 脉冲信号差模辐射的频谱

差模辐射频率特性线



频谱包络线



搜电网  
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中国最大的电子元器件搜索引擎

$$E = 2.6 I A f^2 / D$$

$$E_{\text{dB}} = 20 \lg ( 2.6 I A / D )$$

$+40 \lg f$

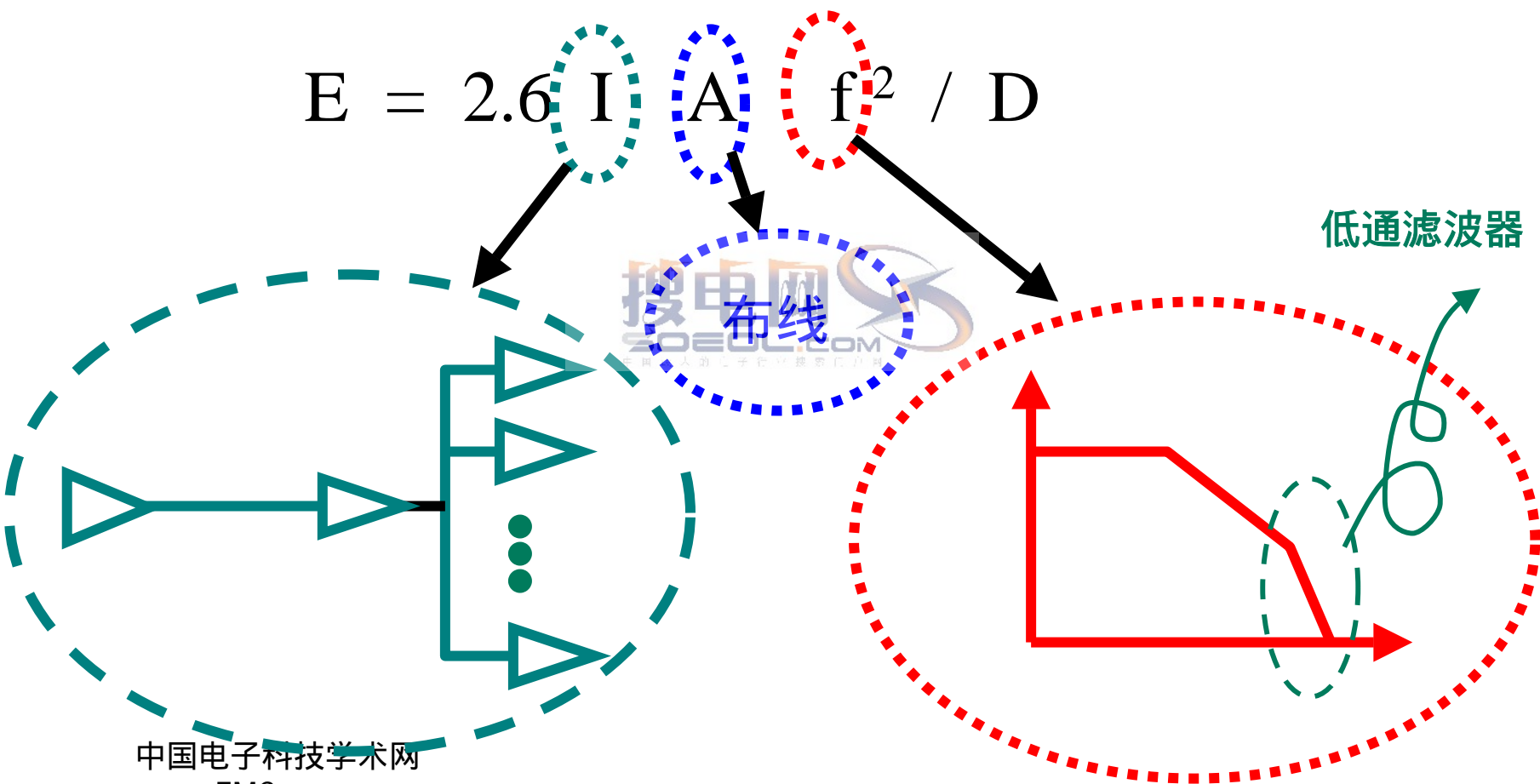
# 不同逻辑电路为了满足EMI指标要求所允许的环路面积

逻辑系列	上升时间	电流	不同时钟频率允许的面积 (cm <sup>2</sup> )			
			4MHz	10	30	100
4000B	40	6	1000	400		
74HC	6	20	50	45	18	6
74LS	6	50	20	18	7.2	2.4
74AC	3.5	80	5.5	2.2	0.75	0.25
74F	3	80	5.5	2.2	0.75	0.25
74AS	1.4	120	2	0.8	3	0.15

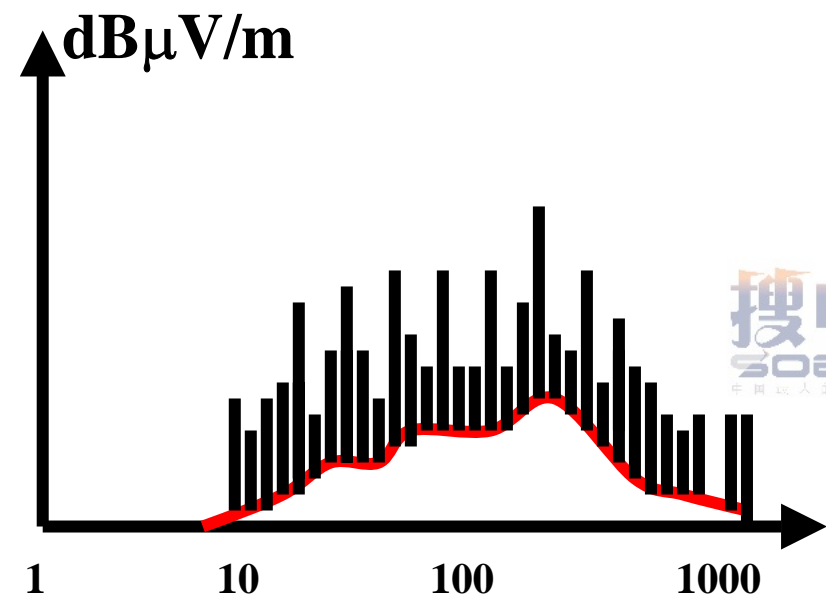
仅代表了一个环路的辐射情况，若有N个环路辐射，乘以 $\sqrt{N}$ 。因此，可能时，分散时钟频率。

# 如何减小差模辐射？

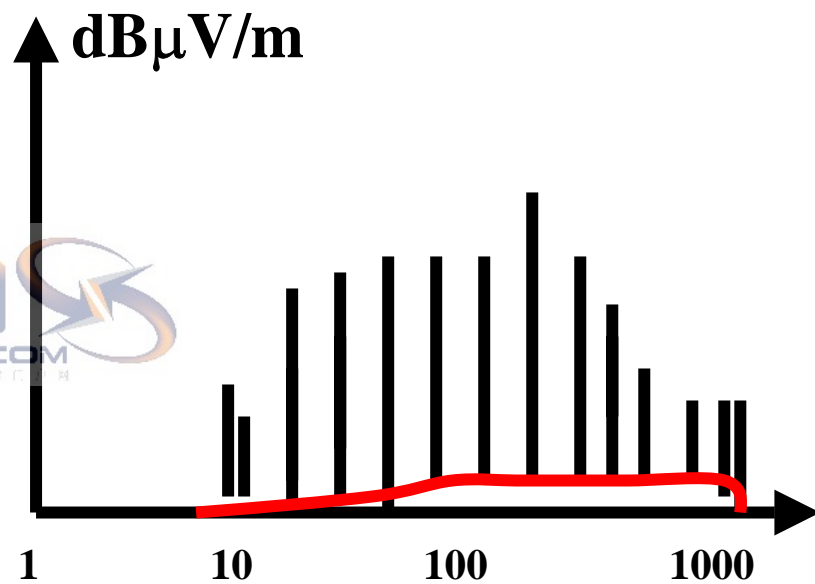
$$E = 2.6 I A f^2 / D$$



# 电路中的强辐射信号

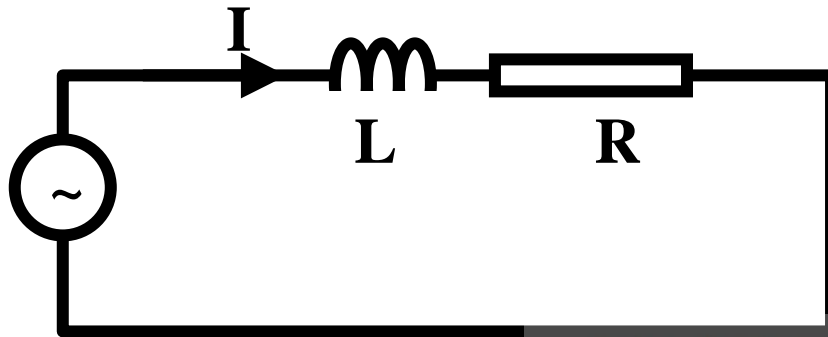


所有电路加电工作



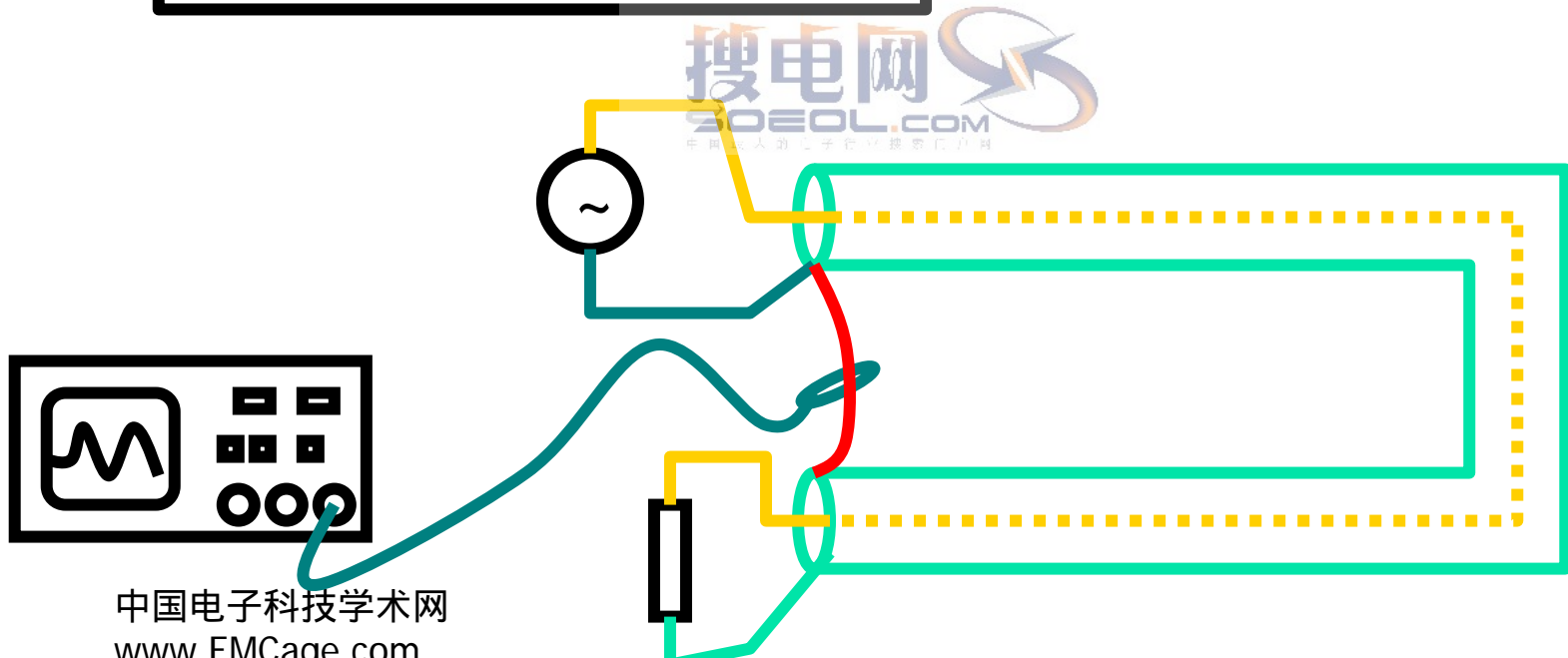
只有时钟电路加电工作

# 电流回路的阻抗

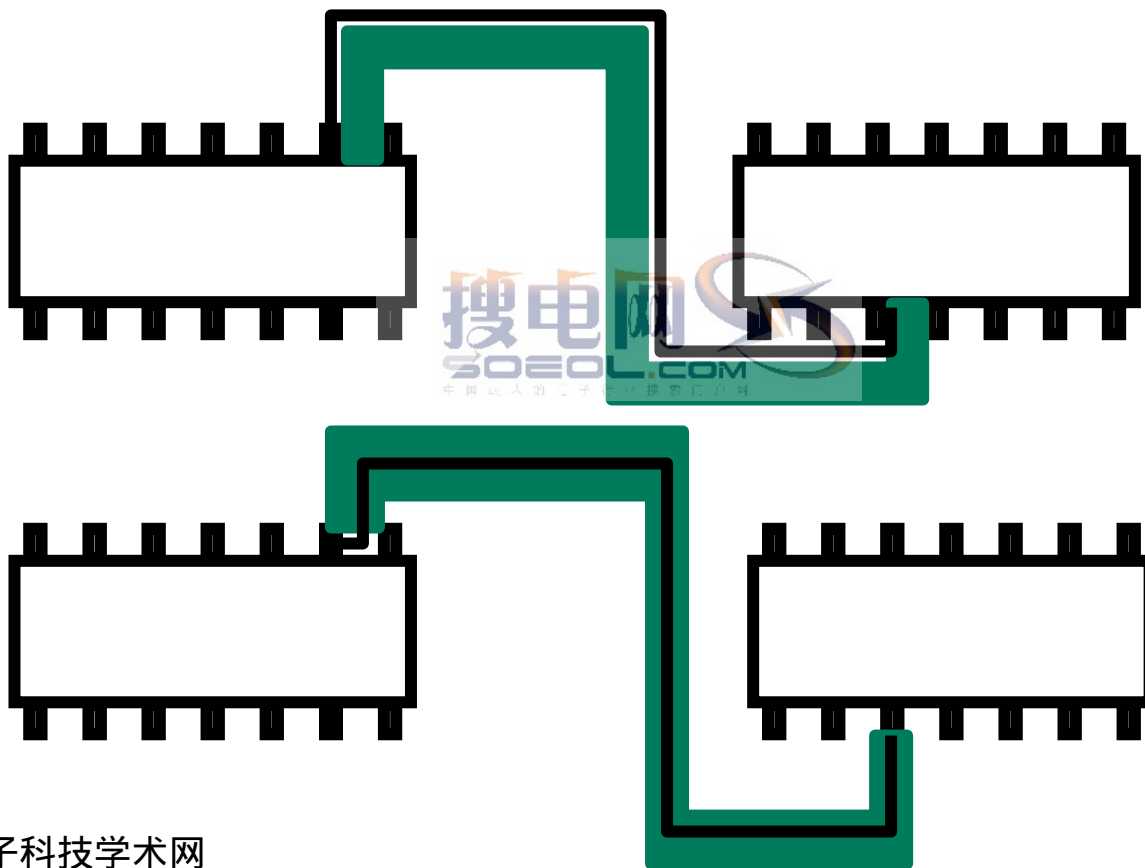


$$Z = R + j\omega L$$

$$L = \Phi / I \quad \Phi \propto A$$

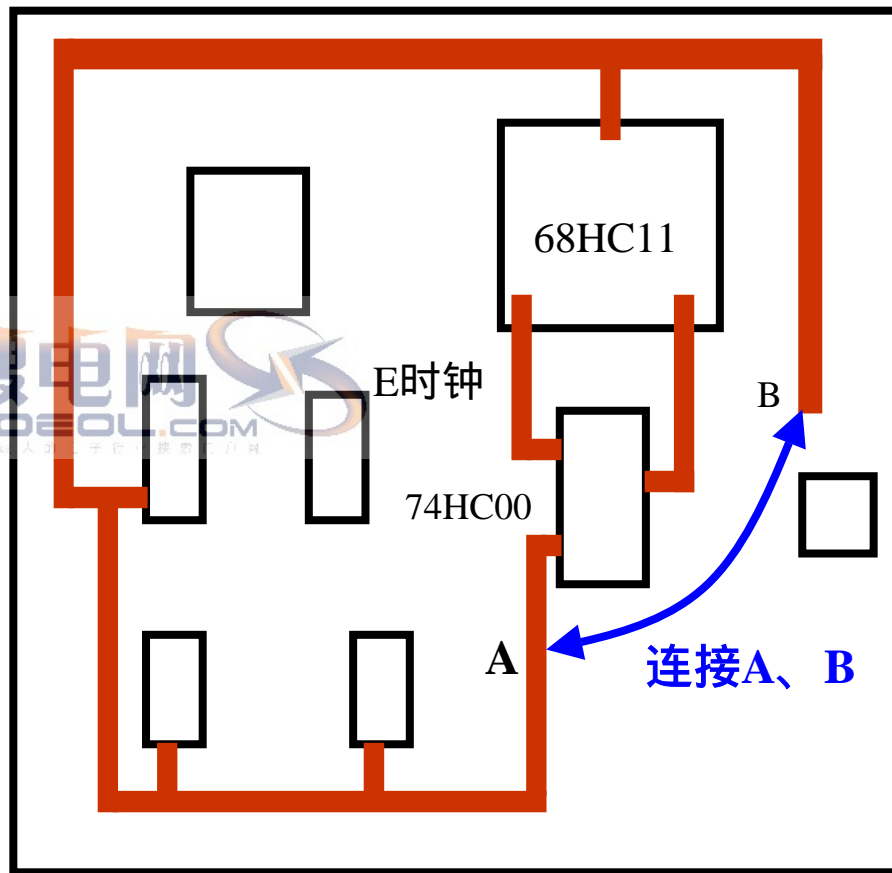
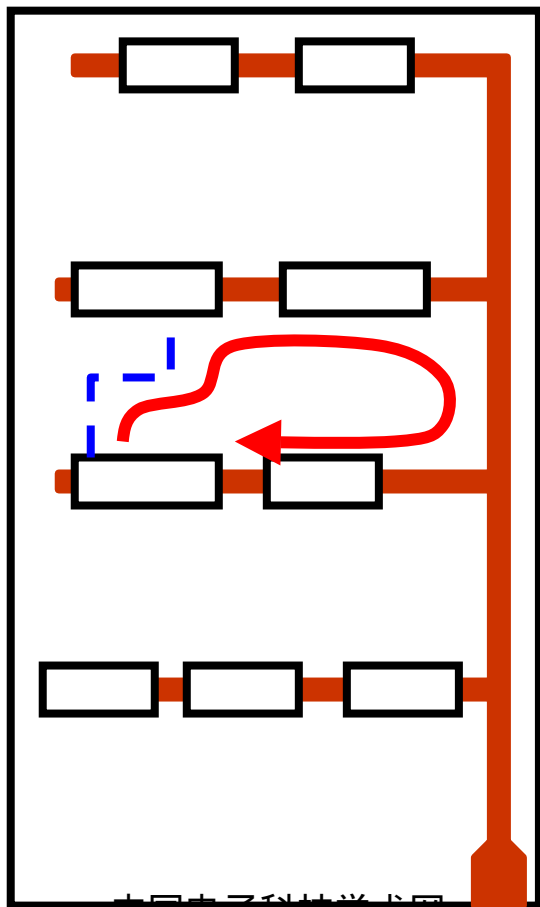


# 单层或双层板如何减小环路的面积

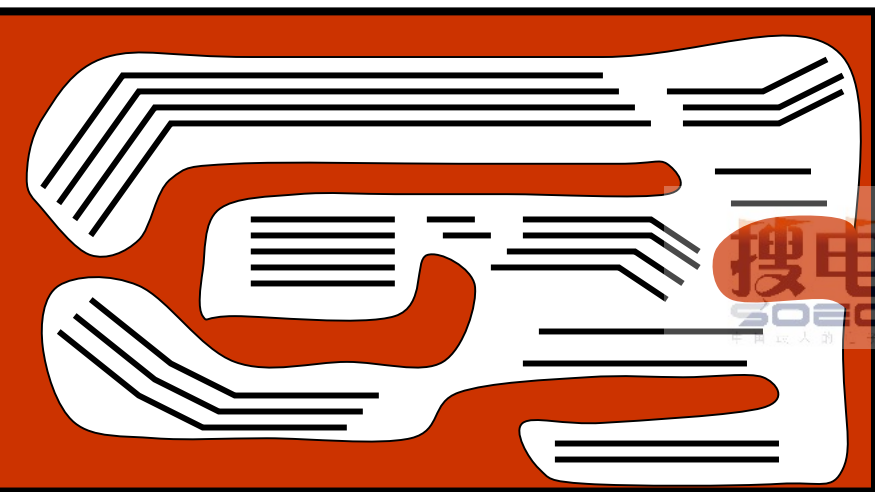




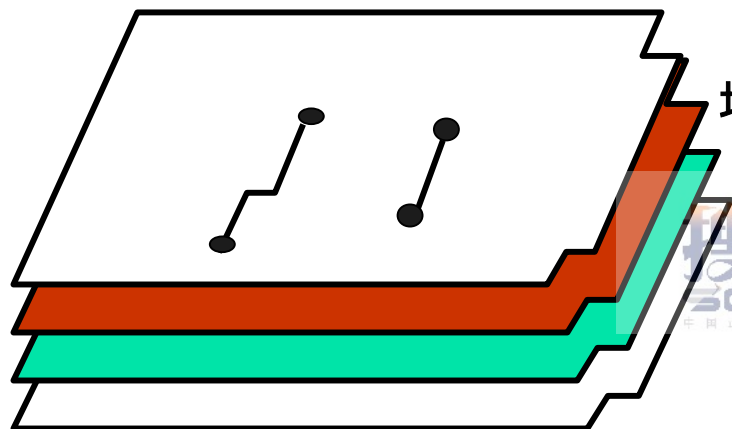
# 不良布线举例



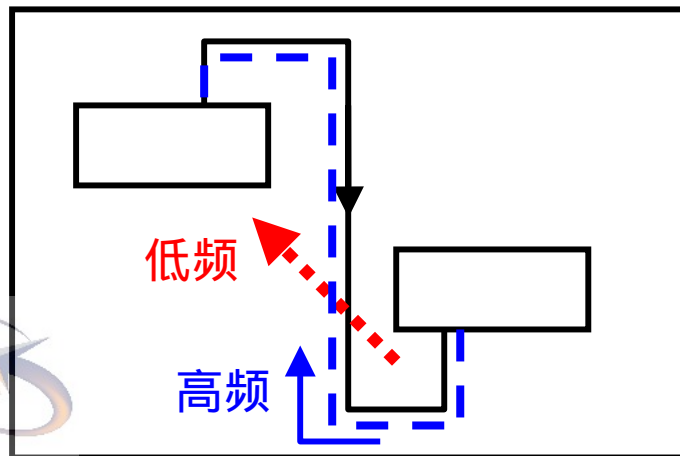
# 随便设置的地线没有用



# 多层板能减小辐射



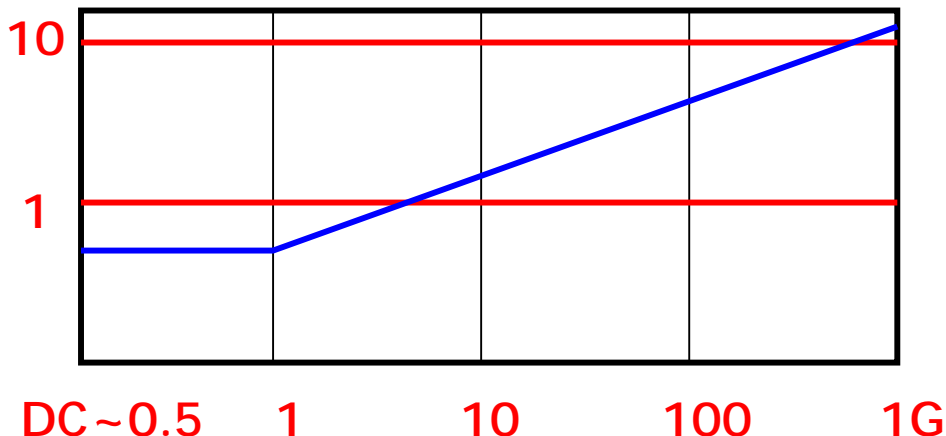
信号1  
电源层  
地线层  
信号2



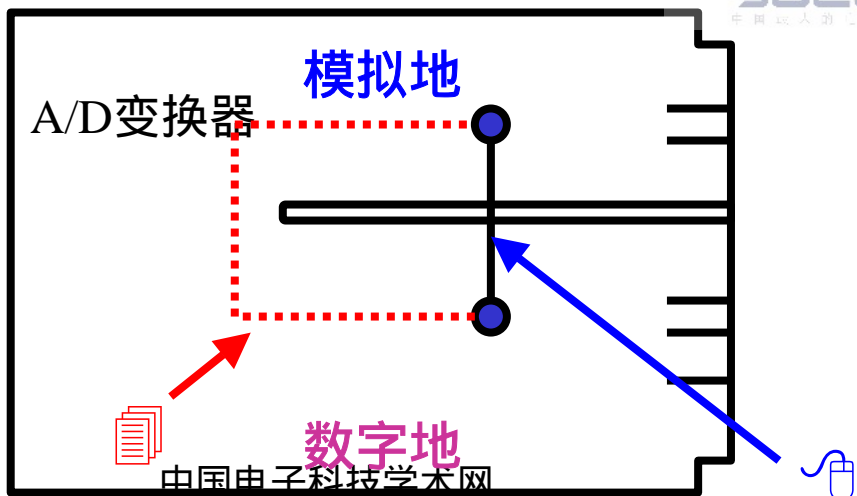
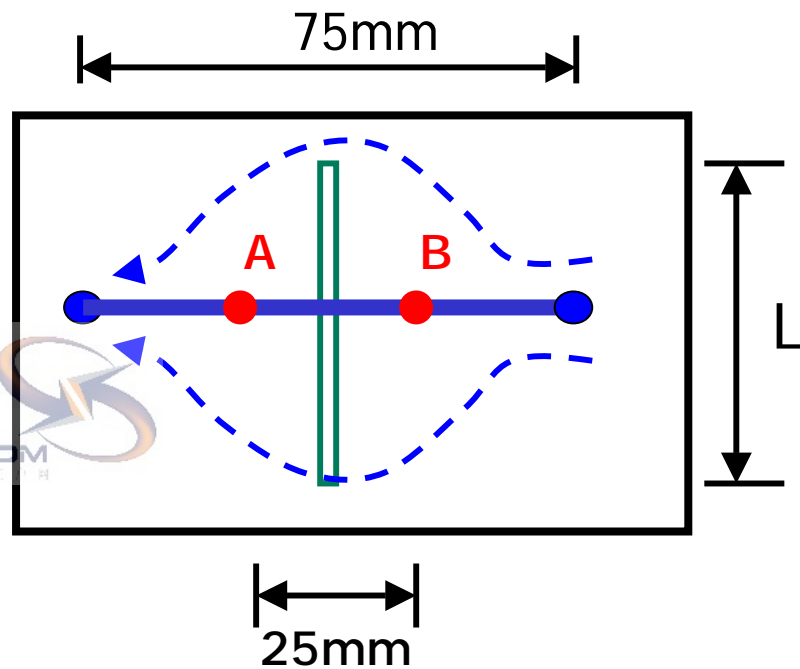
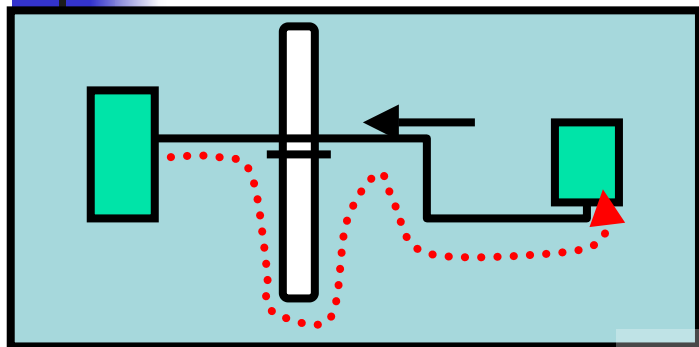
地线面的阻抗,  $m\Omega$ /平方

地线面具有很小的地线阻抗

中国电子科技学术网  
www.FMCage.com



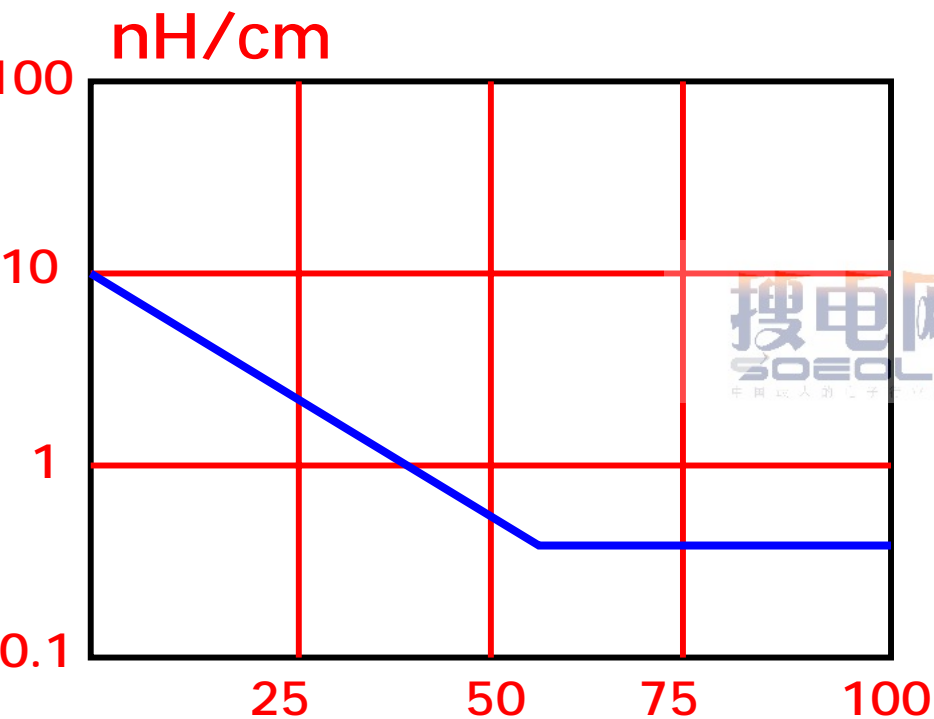
# 地线面上的缝隙的影响



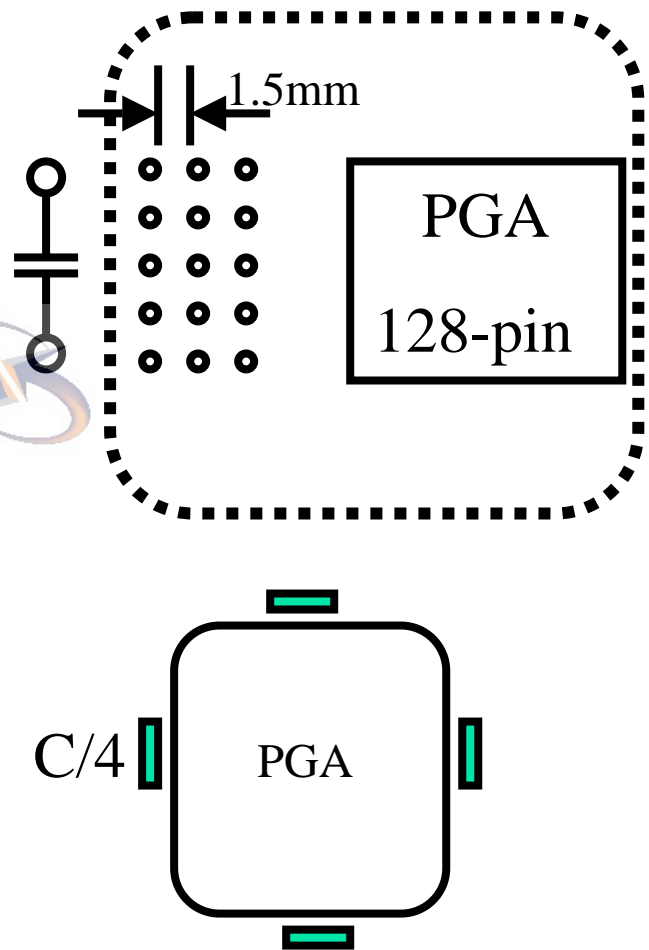
$L : 0 \sim 10\text{cm}$   
 $V_{AB} : 15 \sim 75\text{mV}$

搜电网  
SOEOL.COM  
中国最大的电子行业搜索引擎

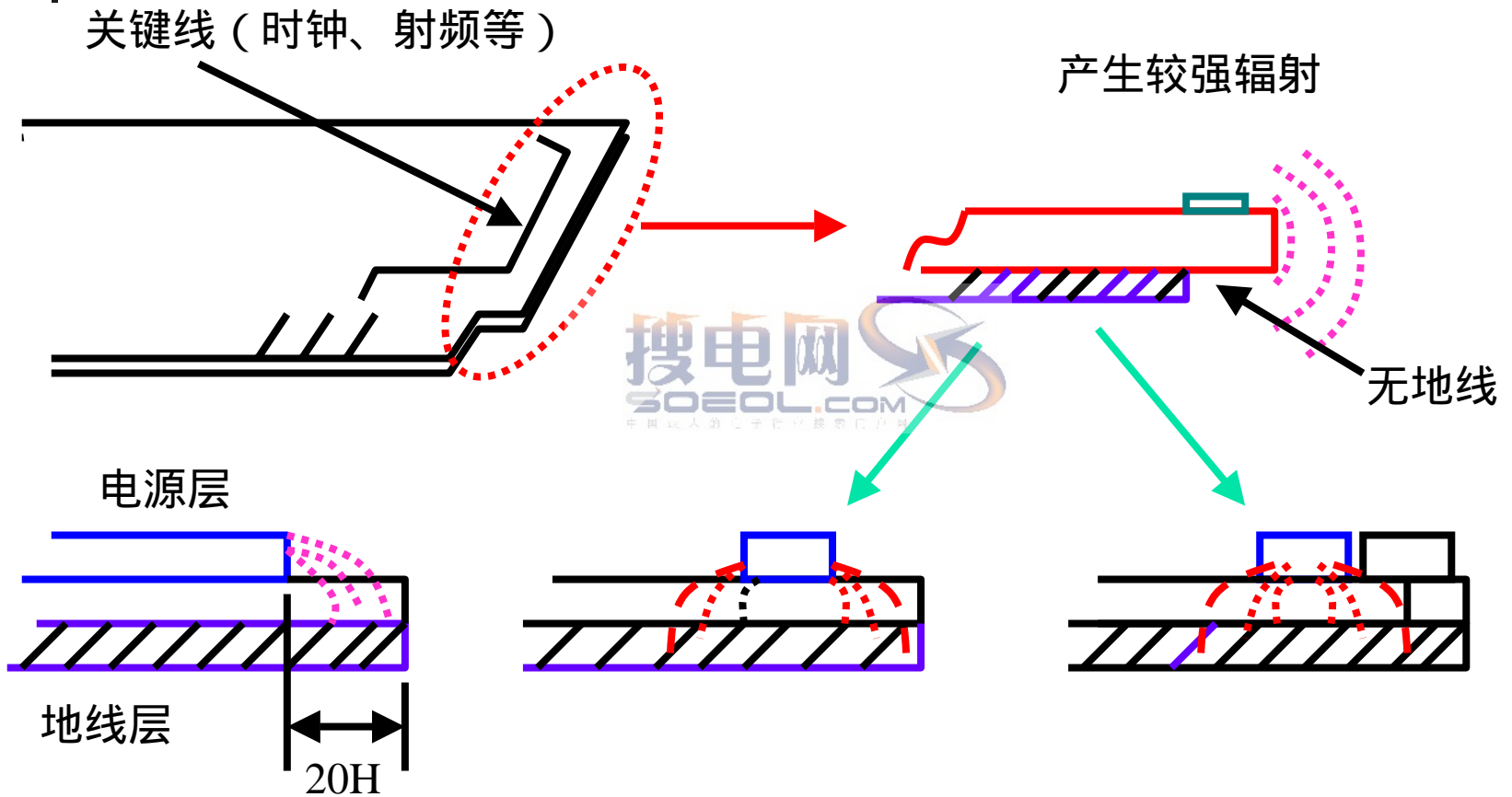
# 过孔的阻抗



与过孔之间的距离 mm



# 线路板边缘的一些问题



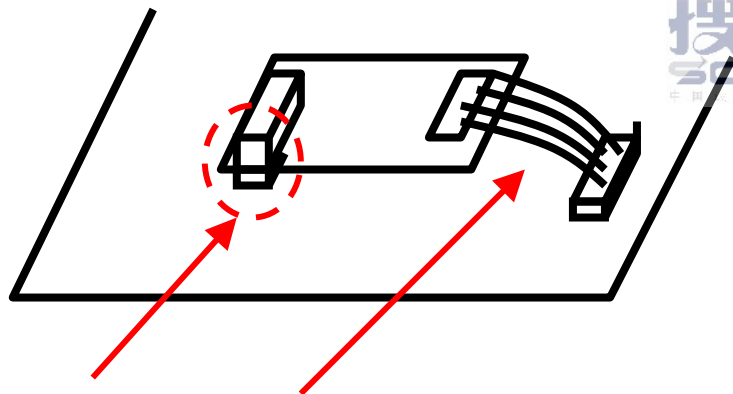
# 扁平电缆的使用

最好

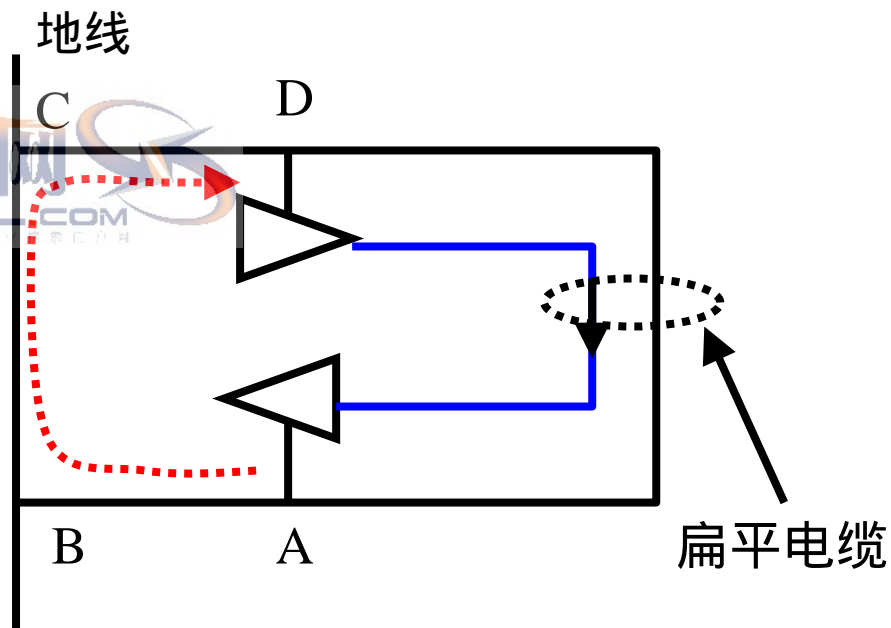
较好

差

较好，但端接困难

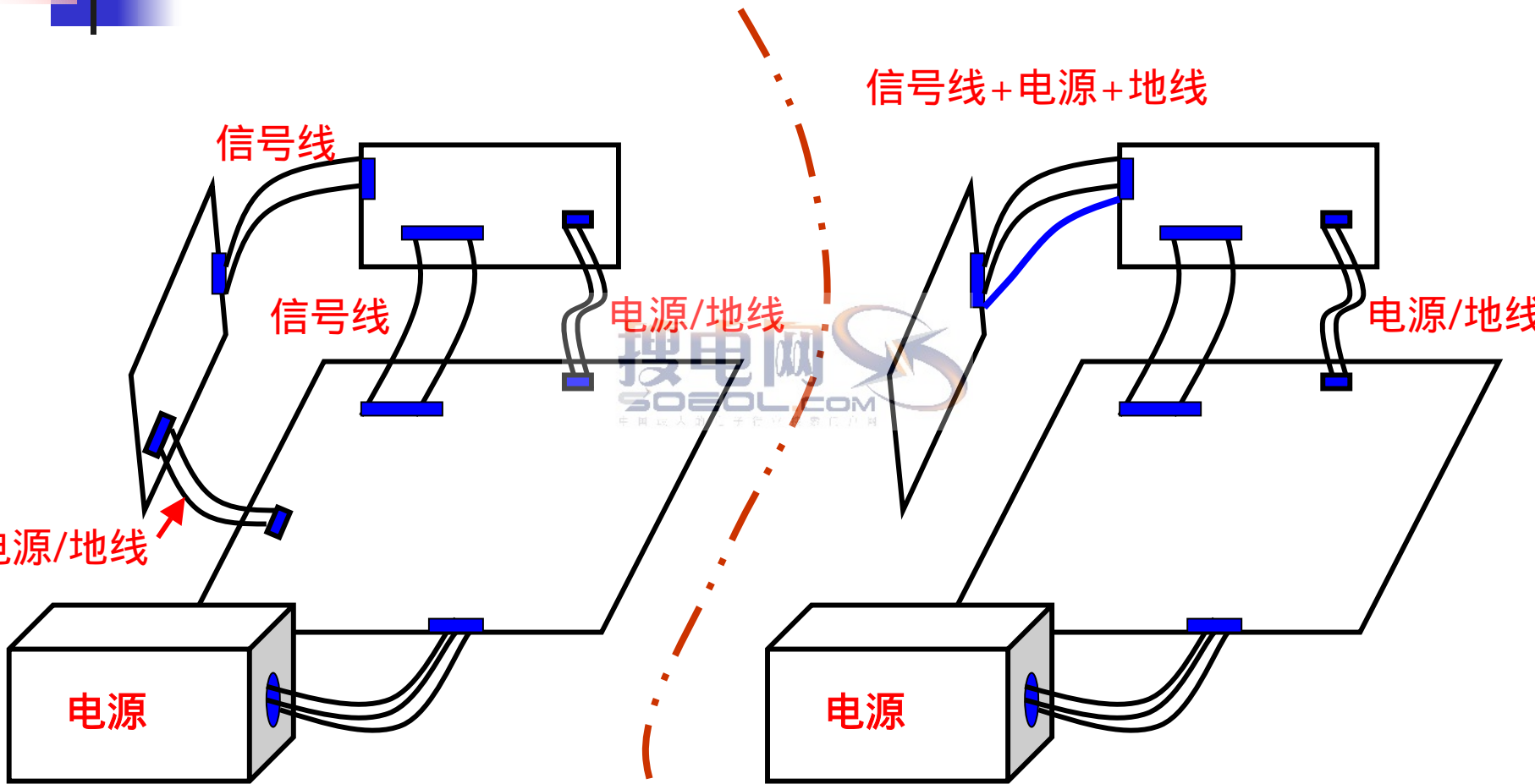


这两处都有地线



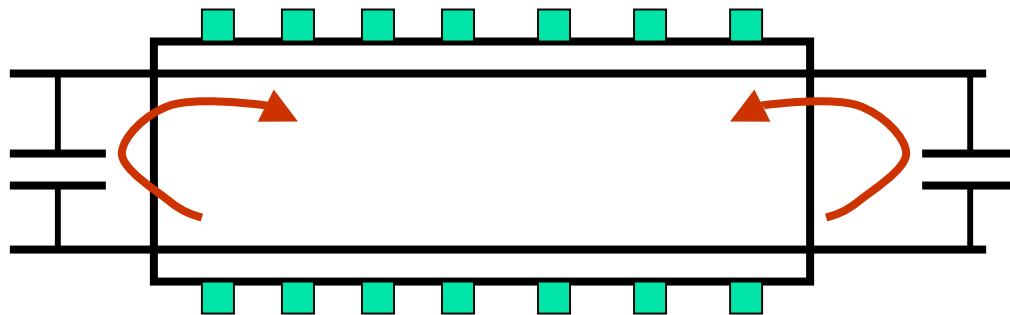
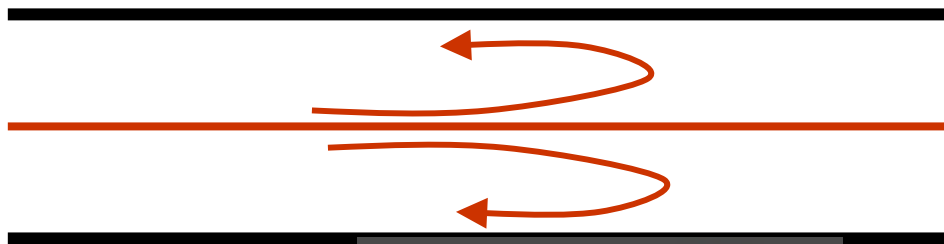
一部分信号回流经过ABCD

# 注意隐蔽的辐射环路

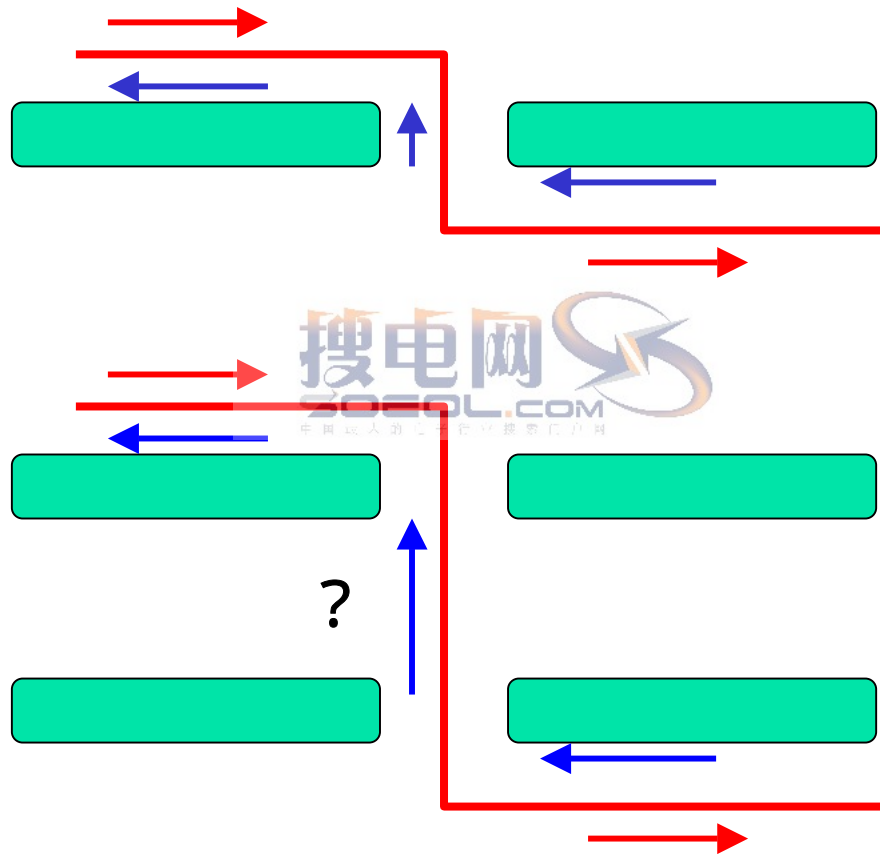




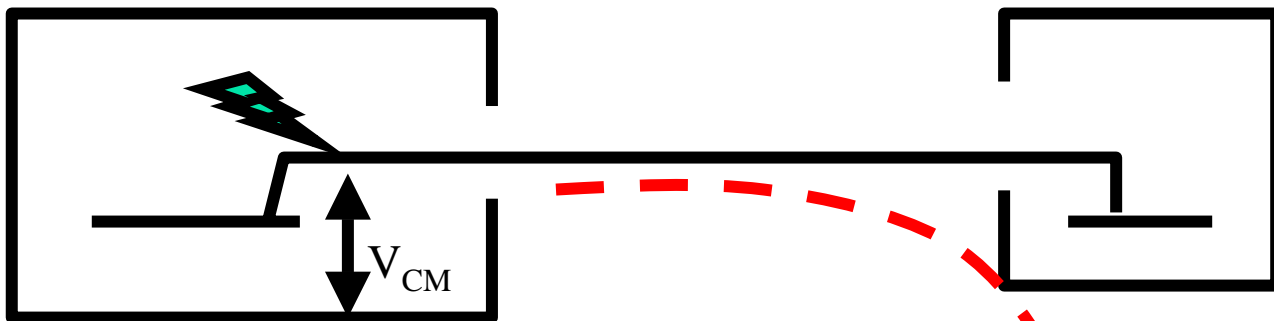
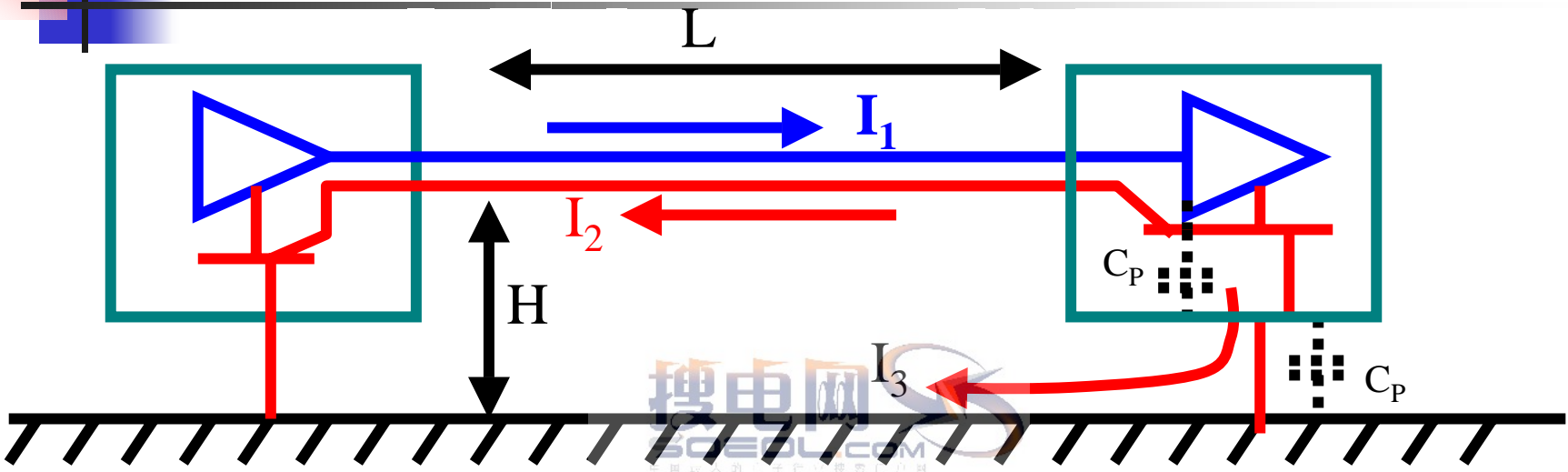
# 环路对消概念减小辐射



# 时钟线避免换层

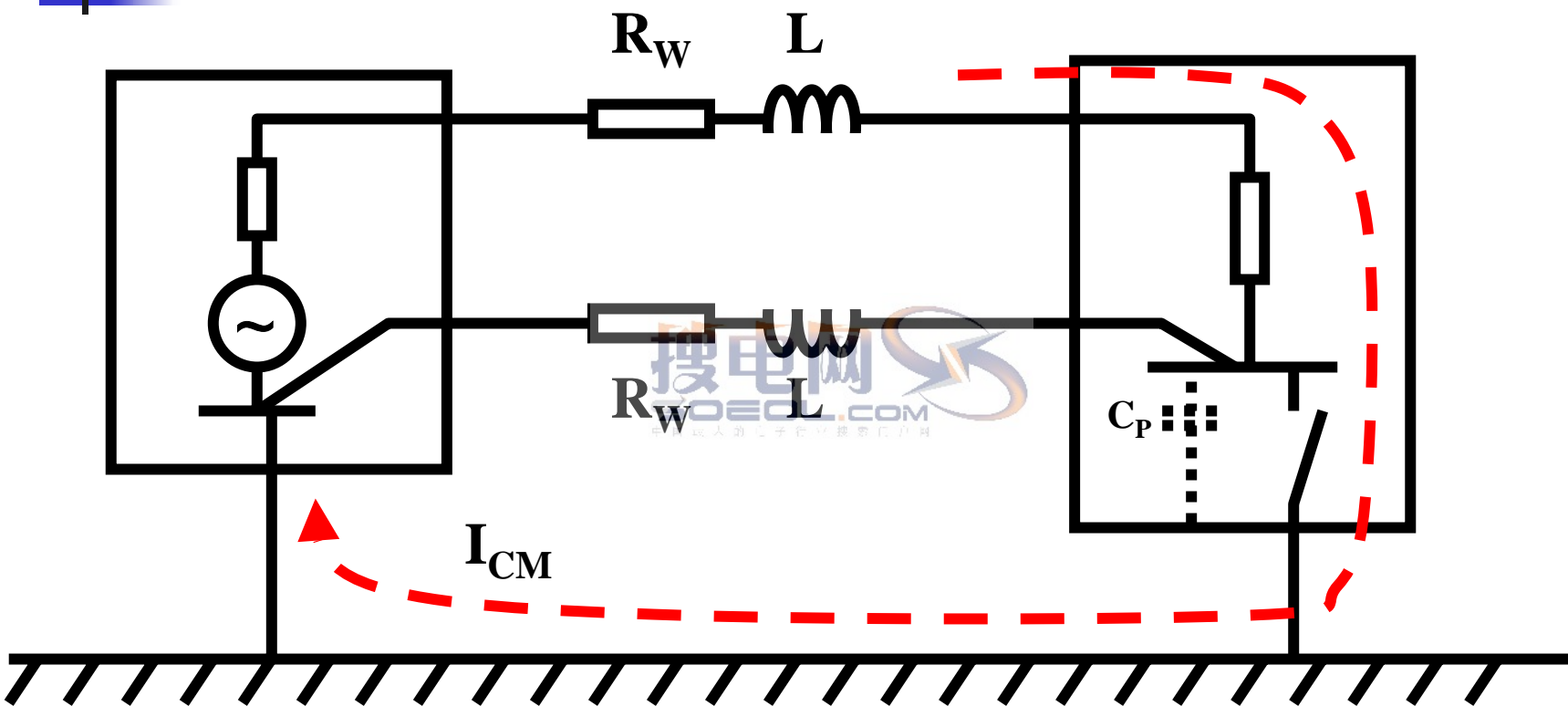


# 外拖电缆的共模辐射



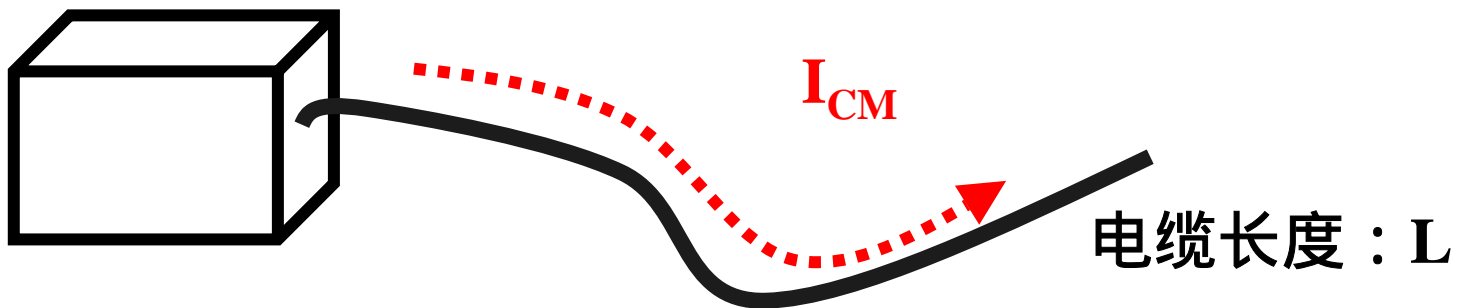
机箱内的  
所有信号  
都会通过  
电缆辐射！

# 两端设备都接地的情况



中国电子科技学术网  $Z_{CM} = R_W + j\omega L + R_L + 1/j\omega C$   
www.FMCage.com

# 悬浮电缆



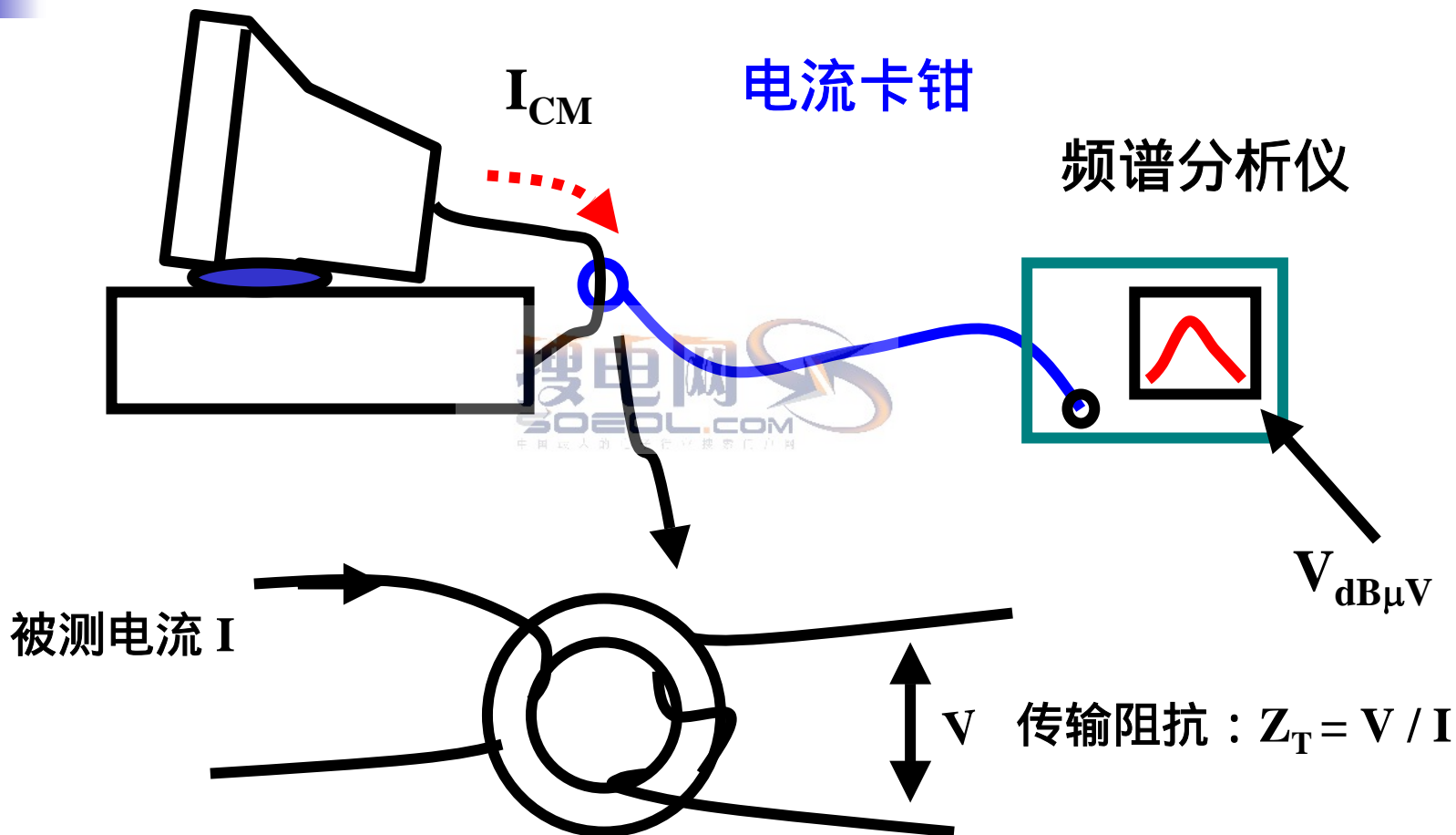
近场区内:  $E = 1430 I L / (f D^3)$   $\mu V/m$

远场区内:  $E = 0.63 I L f / D$   $\mu V/m$

考虑地面反射:  $E = 1.26 I L f / D$   $\mu V/m$

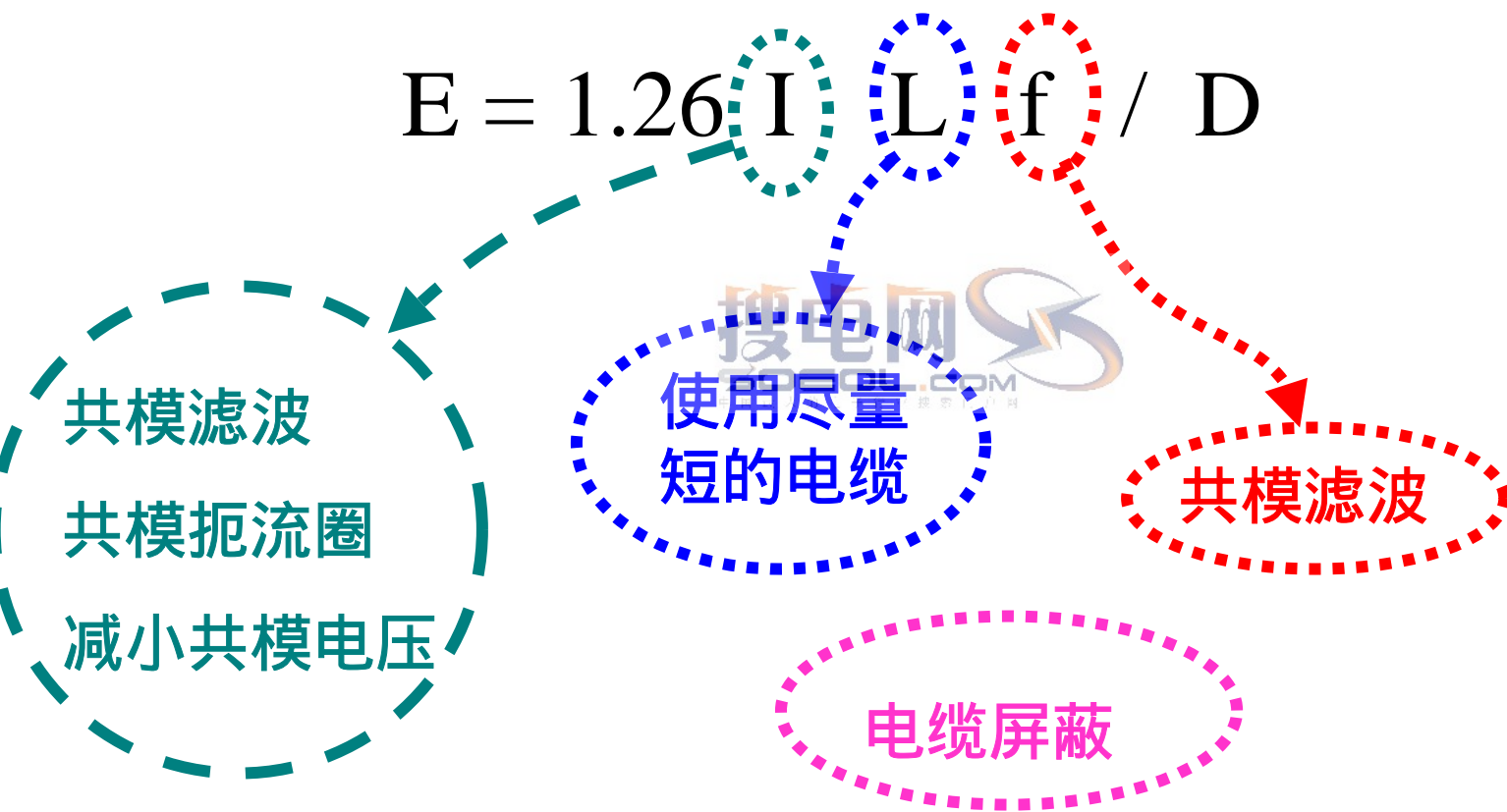
$L > \lambda/2$ 或 $\lambda/4$ 时:  $E = 120 I / D$   $\mu V/m$

# 共模电流的测量

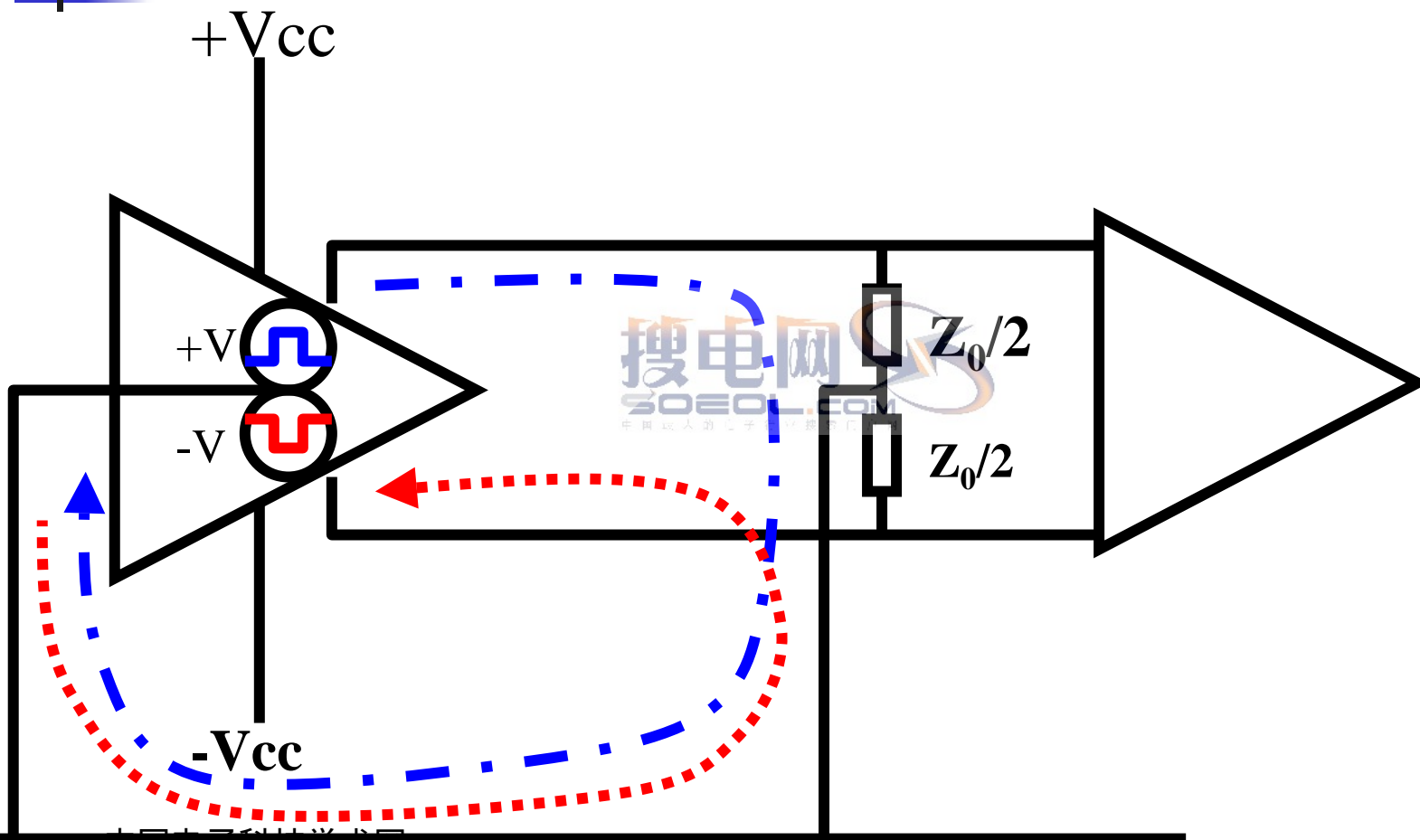


# 怎样减小共模辐射

$$E = 1.26 I L f / D$$

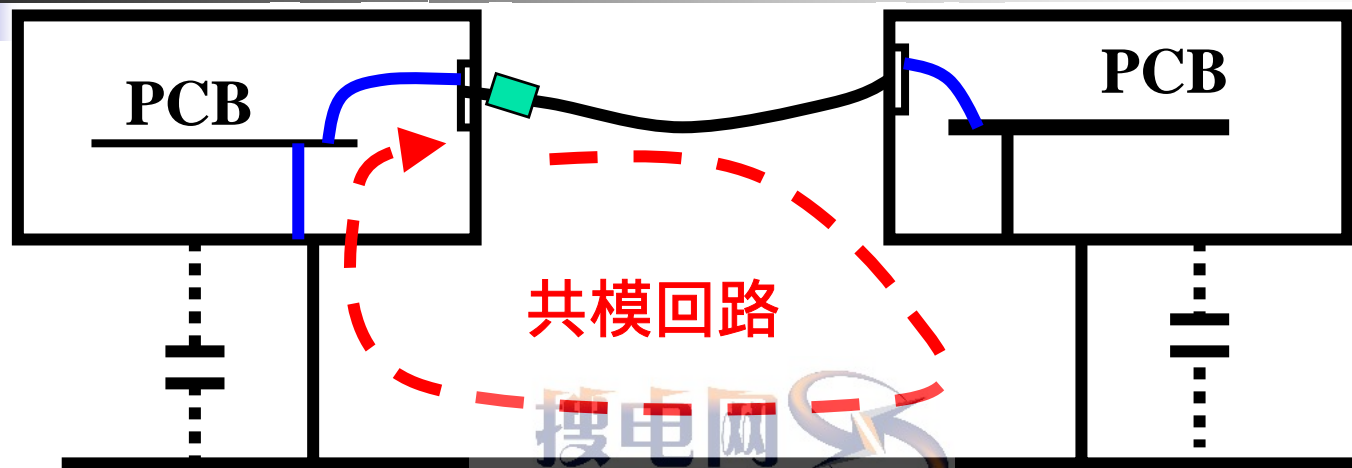


# 平衡接口电路



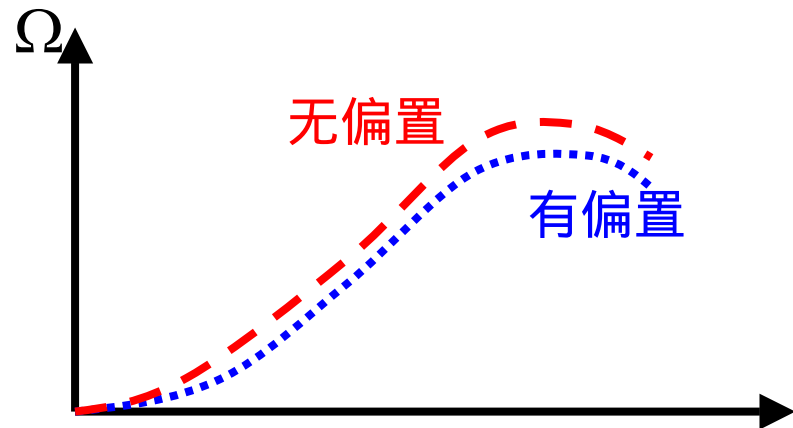
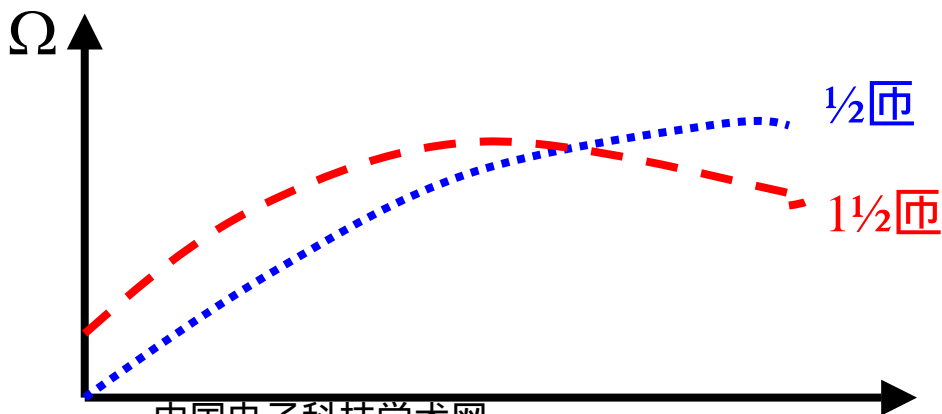
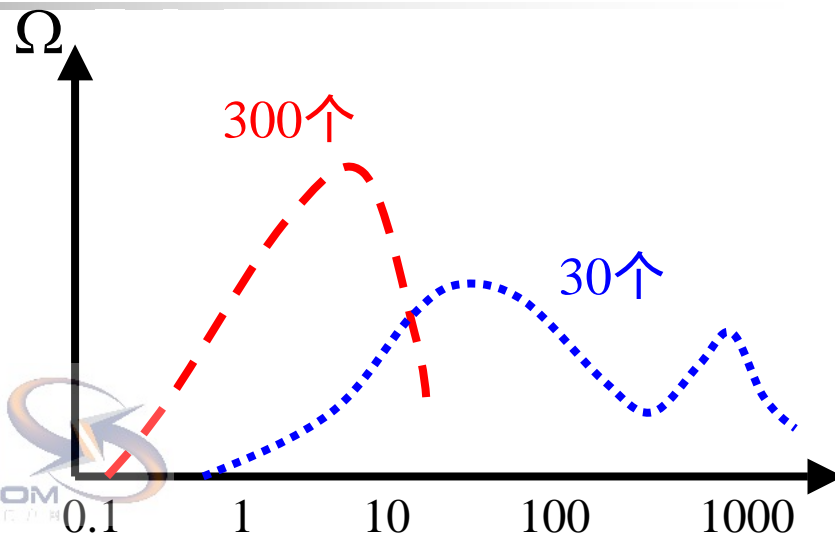
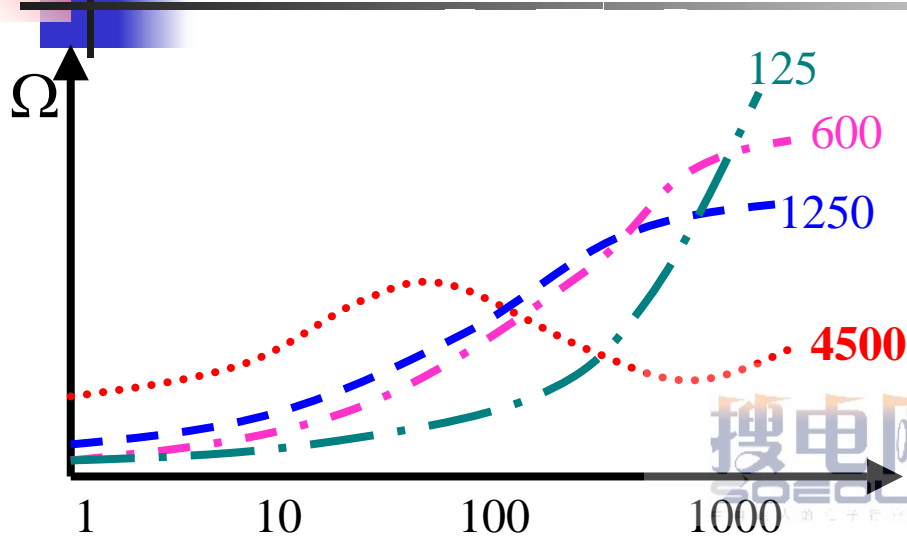


# 增加共模回路的阻抗

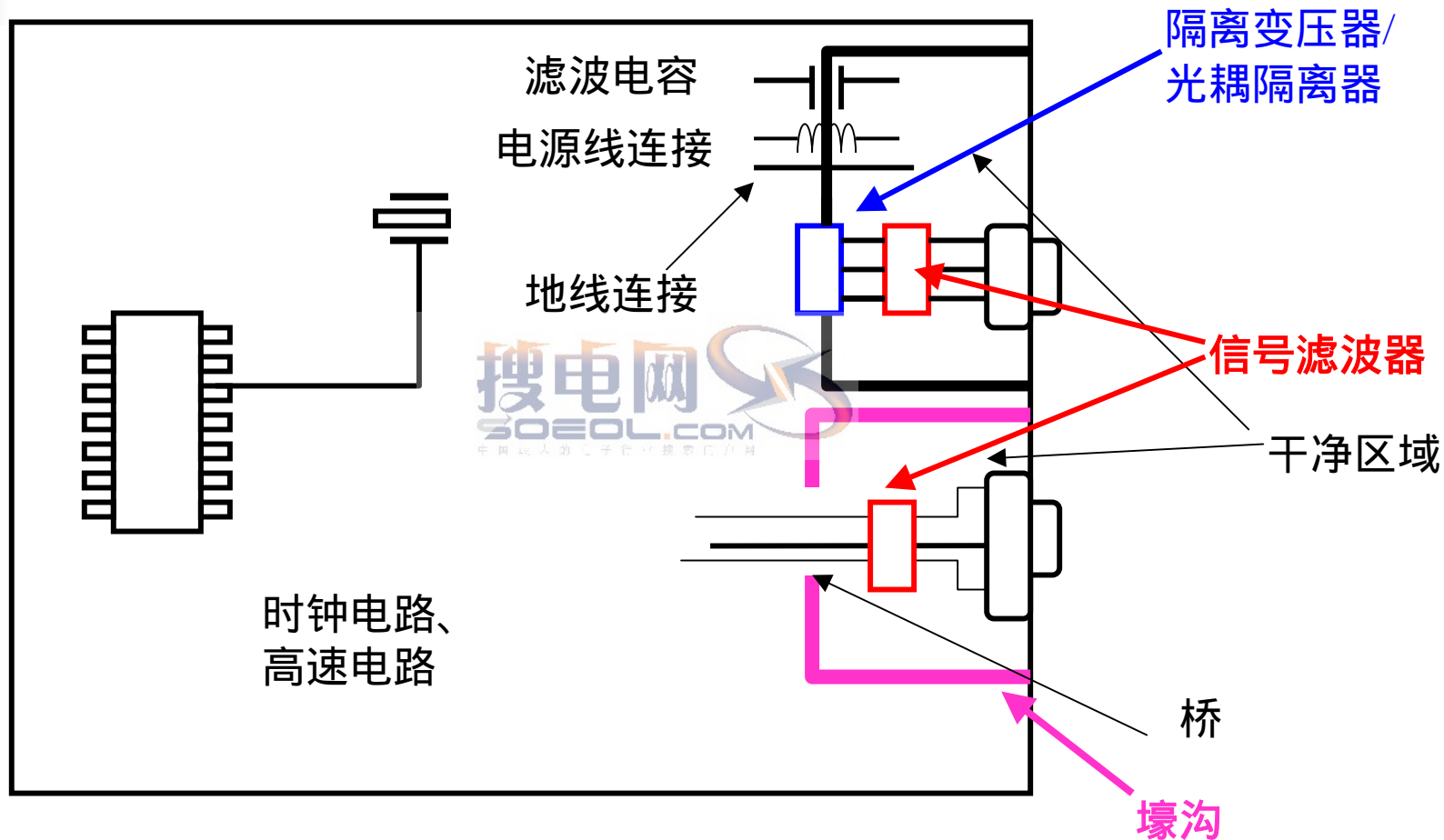


$$\begin{aligned} \text{改善量} &= 20\lg(E_1 / E_2) = 20\lg(I_{CM1} / I_{CM2}) \\ &= 20\lg[(V_{CM} / Z_{CM1}) / (V_{CM} / Z_{CM2})] \\ &= 20\lg(Z_{CM2} / Z_{CM1}) \\ &= 20\lg(1 + Z_L / Z_{CM1}) \quad \text{dB} \end{aligned}$$

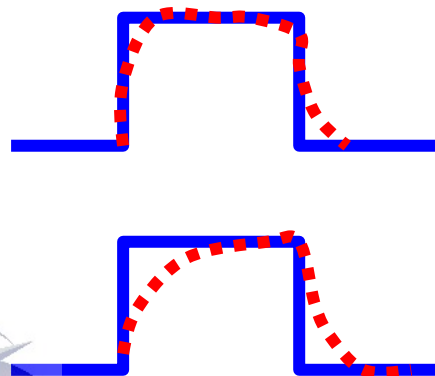
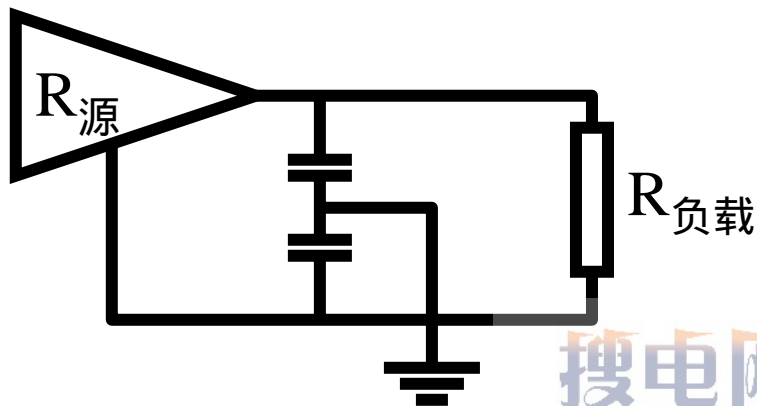
# 铁氧体磁环使用方面的一些问题



# I/O接口布线的一些要点

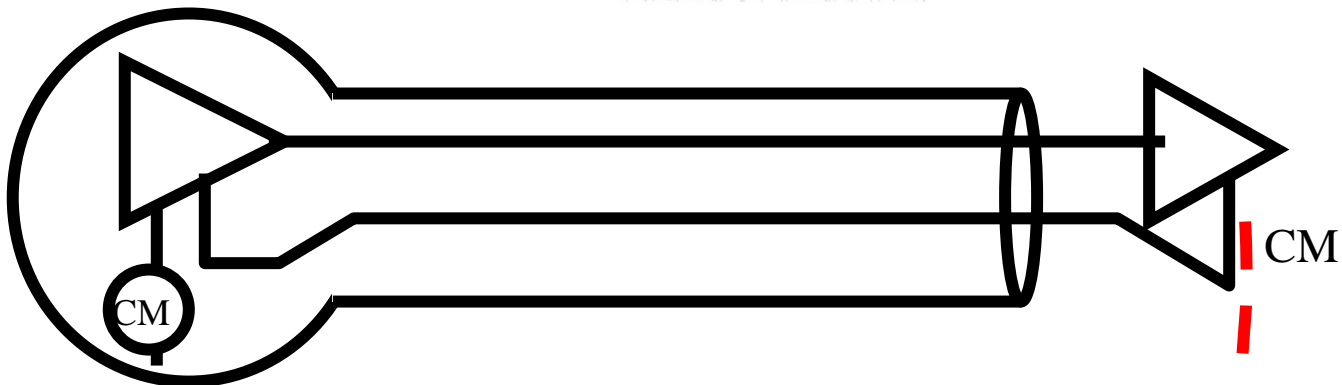
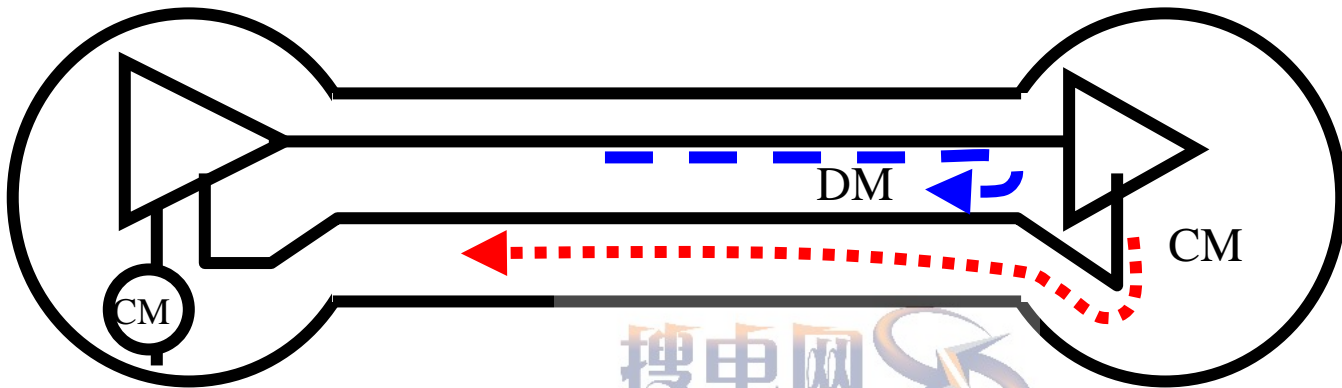


# 滤波器电容量的选择

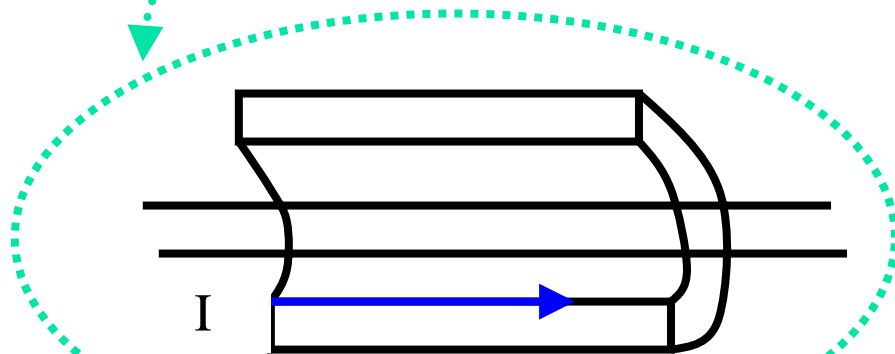
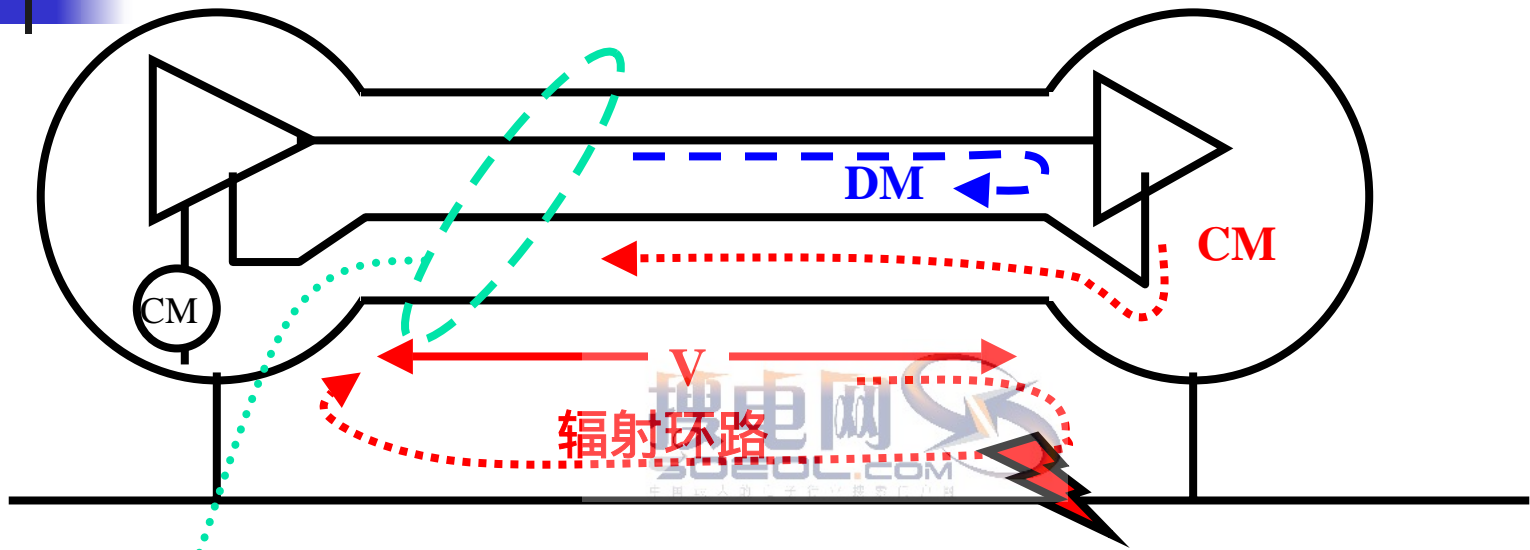


	低速接口 10 ~ 100kB/s	高速接口 2MB/s	低速CMOS	TTL
上升时间 $t_r$	0.5 ~ 1 $\mu$ s	50ns	100ns	10ns
带宽 BW	320kHz	6MHz	3.2MHz	32MHz
总阻抗 R	120 $\Omega$	100 $\Omega$	300 $\Omega$	100 ~ 150 $\Omega$
最大电容 C	2400pF	150pF	100pF	30pF

# 用屏蔽电缆抑制共模辐射

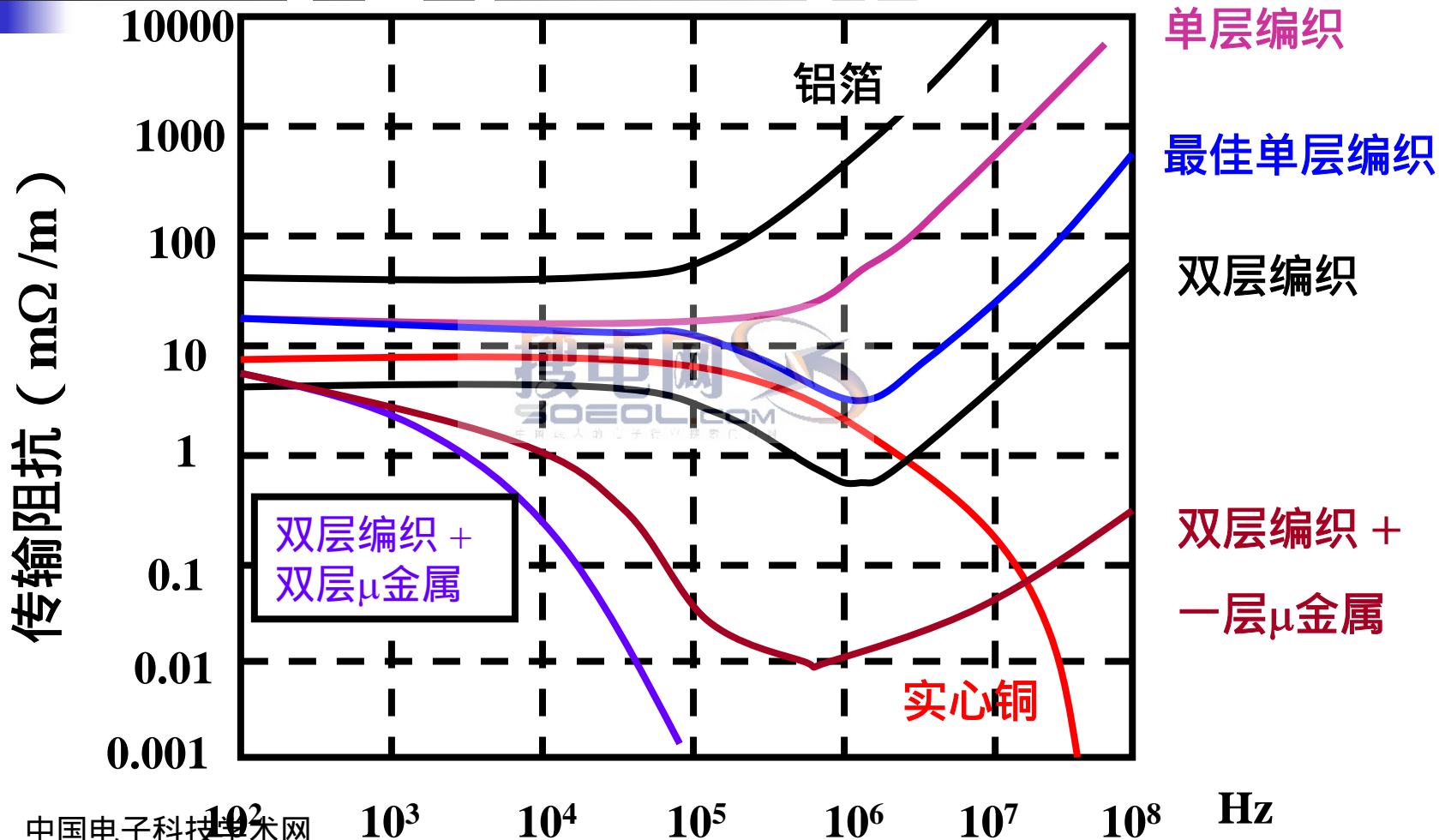


# 屏蔽电缆的评估

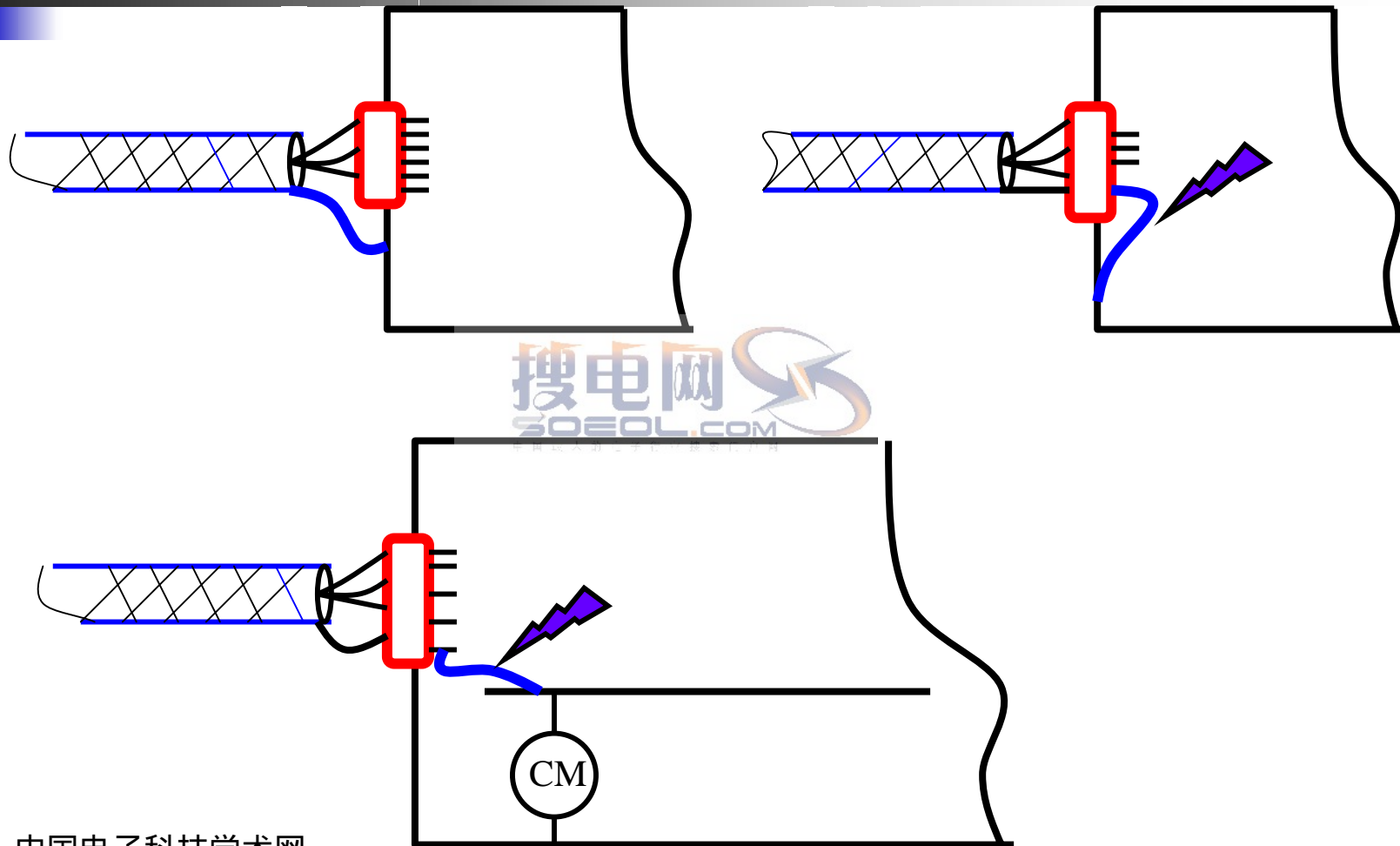


$$Z_T = V / I$$

# 不同屏蔽层的传输阻抗



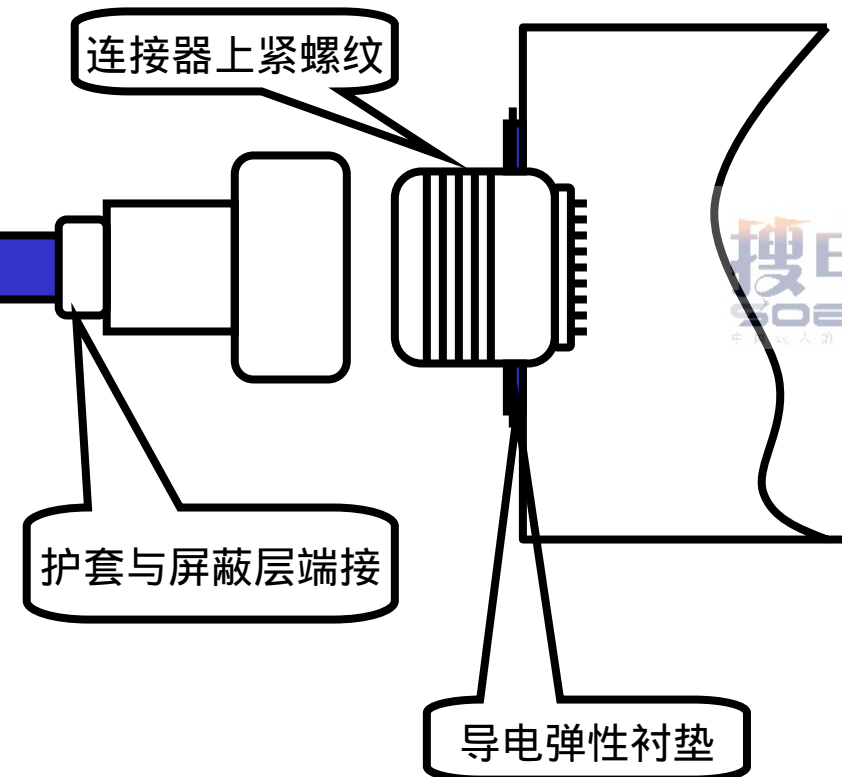
# 屏蔽层的错误接法



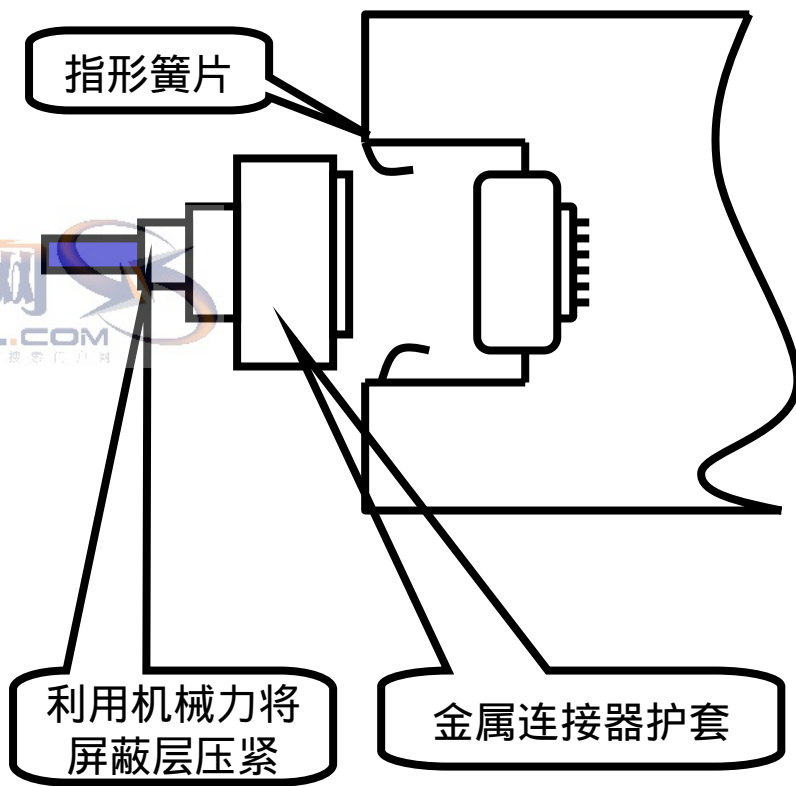


# 电缆屏蔽层的正确端接

## 航空连接器



## D形连接器



# D型连接器的屏蔽层搭接

“Dimpled” D-type connector body makes multiple bonds all around when mated

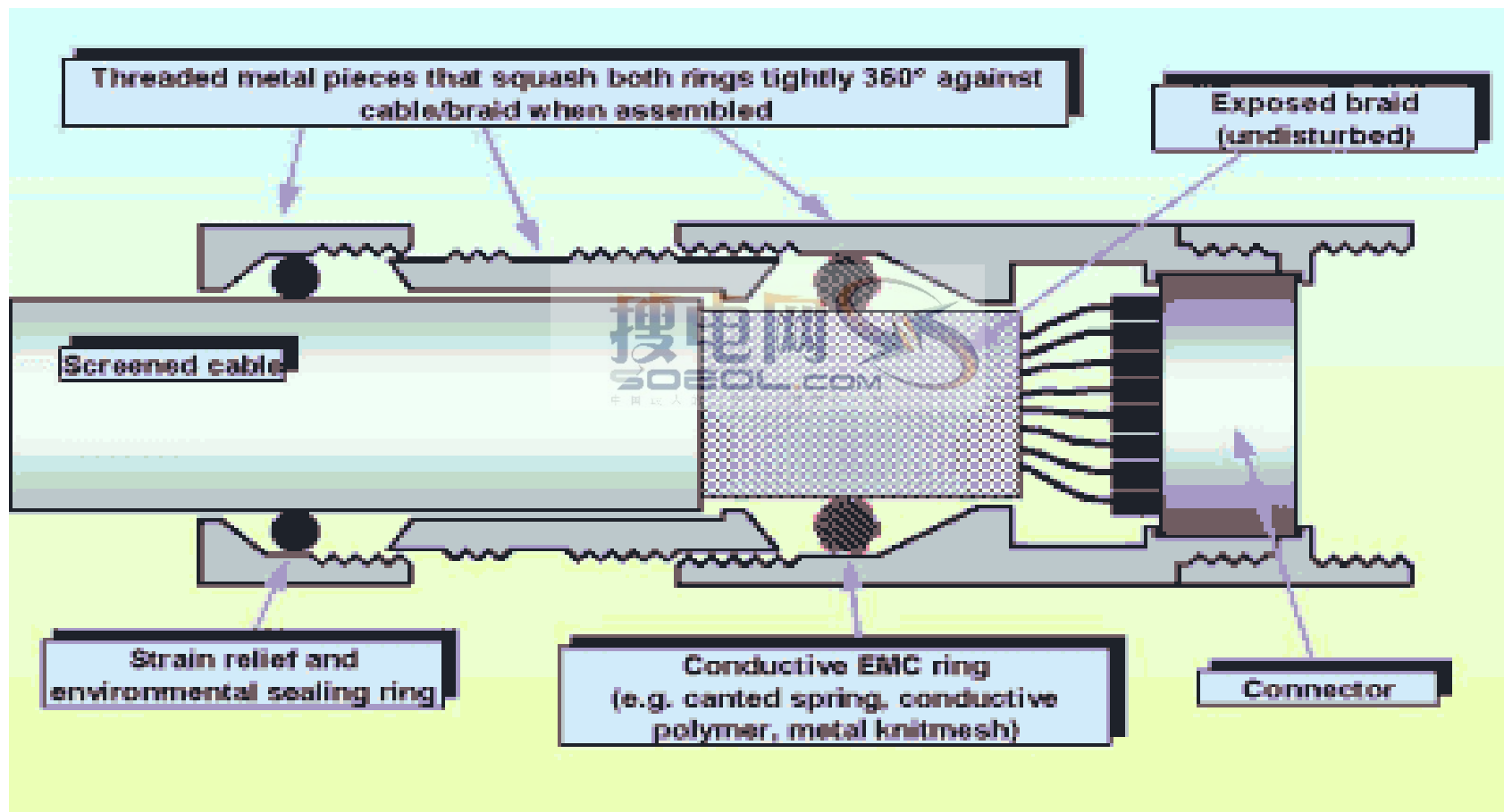
Metal (or metallised) backshell

Screen exposed and 360° clamped, preferably undisturbed (must be a tight fit)

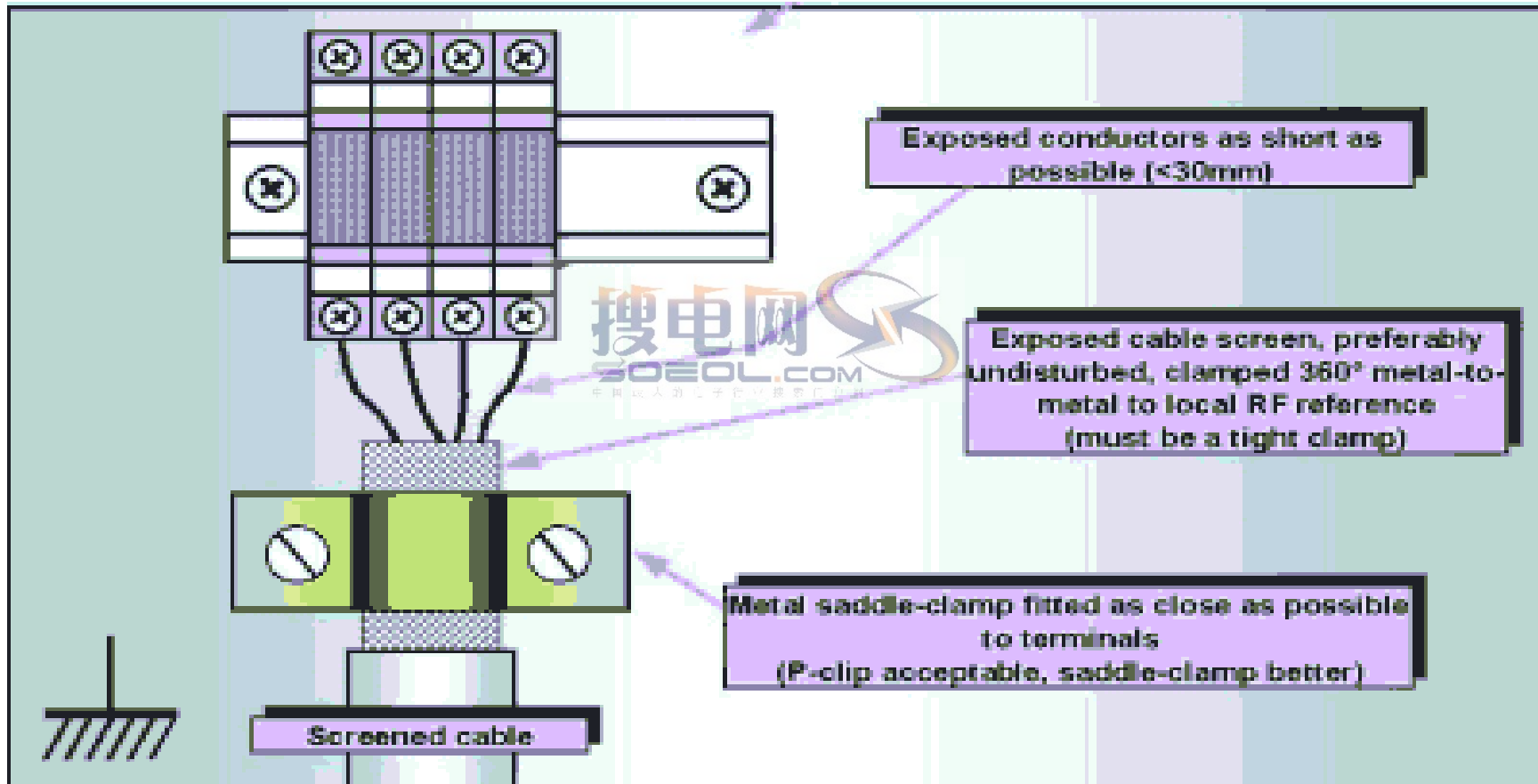
Other 360° bonding methods and 360° shielded connectors are also acceptable if basic requirements are met



# 圆形连接器屏蔽层搭接



# 接线端子上的屏蔽电缆



# 尽量减小小辫接法的危害

Pigtails are very poor for EMC

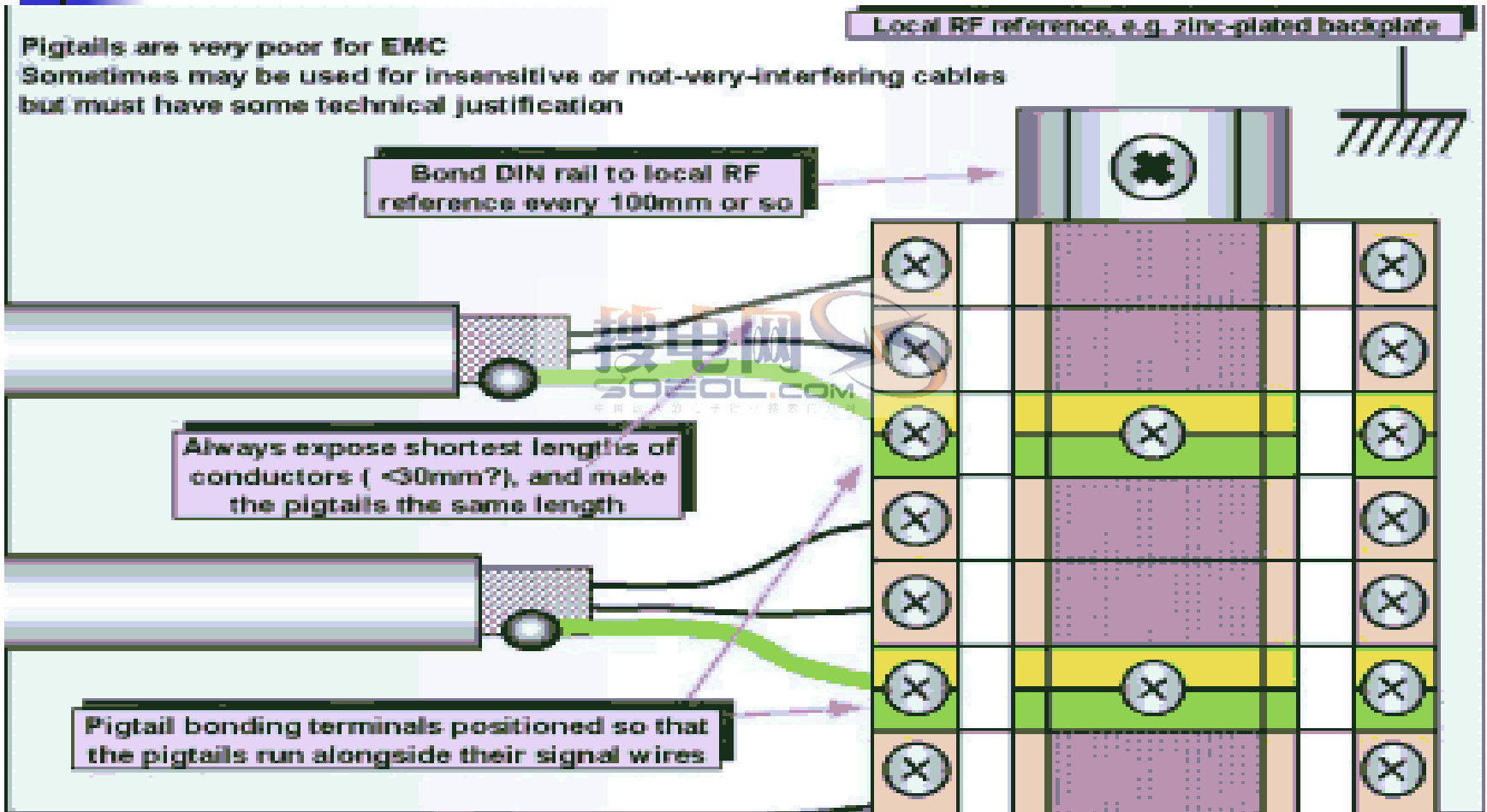
Sometimes may be used for insensitive or not-very-interfering cables but must have some technical justification

Bond DIN rail to local RF reference every 100mm or so

Local RF reference, e.g. zinc-plated backplate

Always expose shortest lengths of conductors (<30mm?), and make the pigtails the same length

Pigtail bonding terminals positioned so that the pigtails run alongside their signal wires



# 线路板上的局部屏蔽

