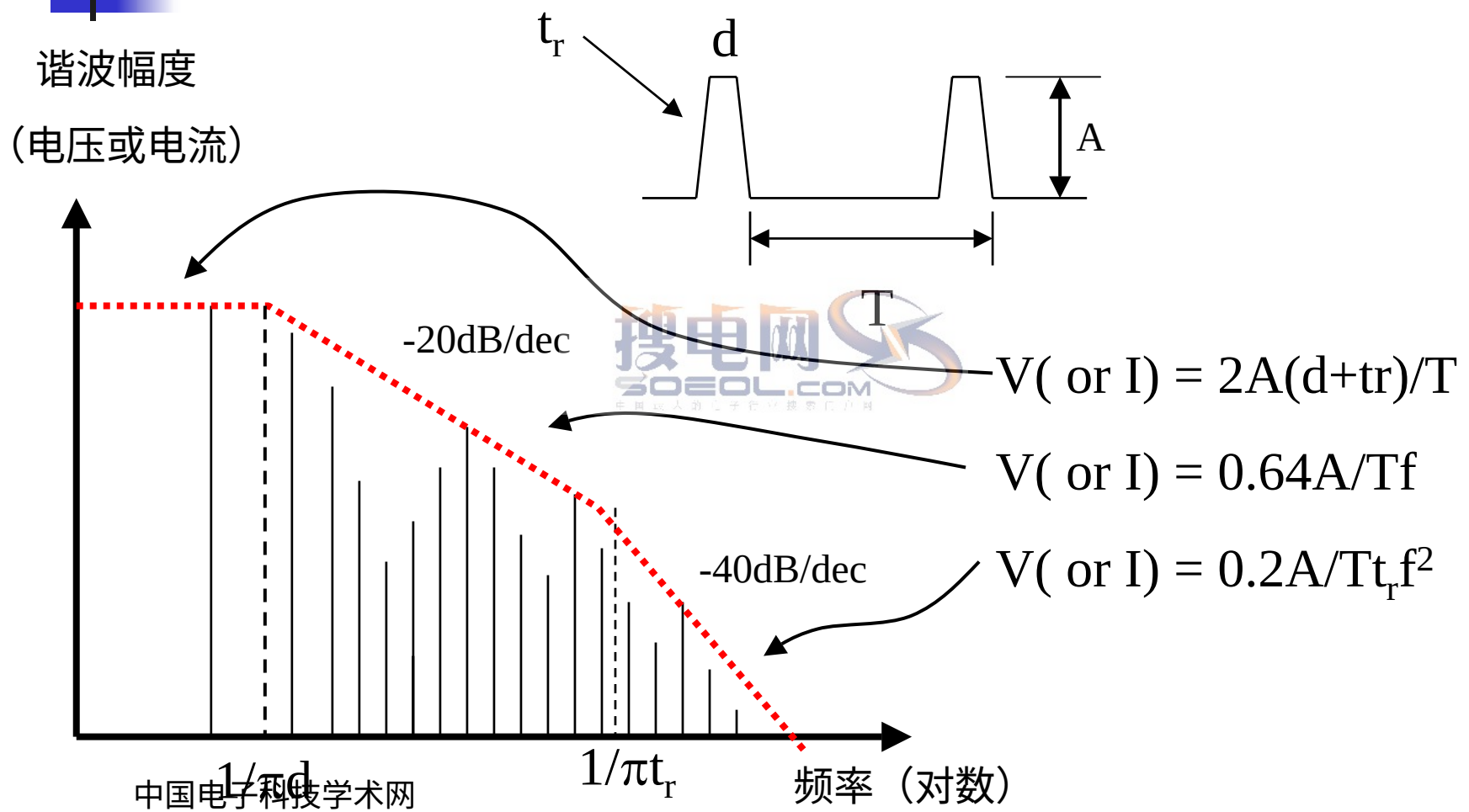
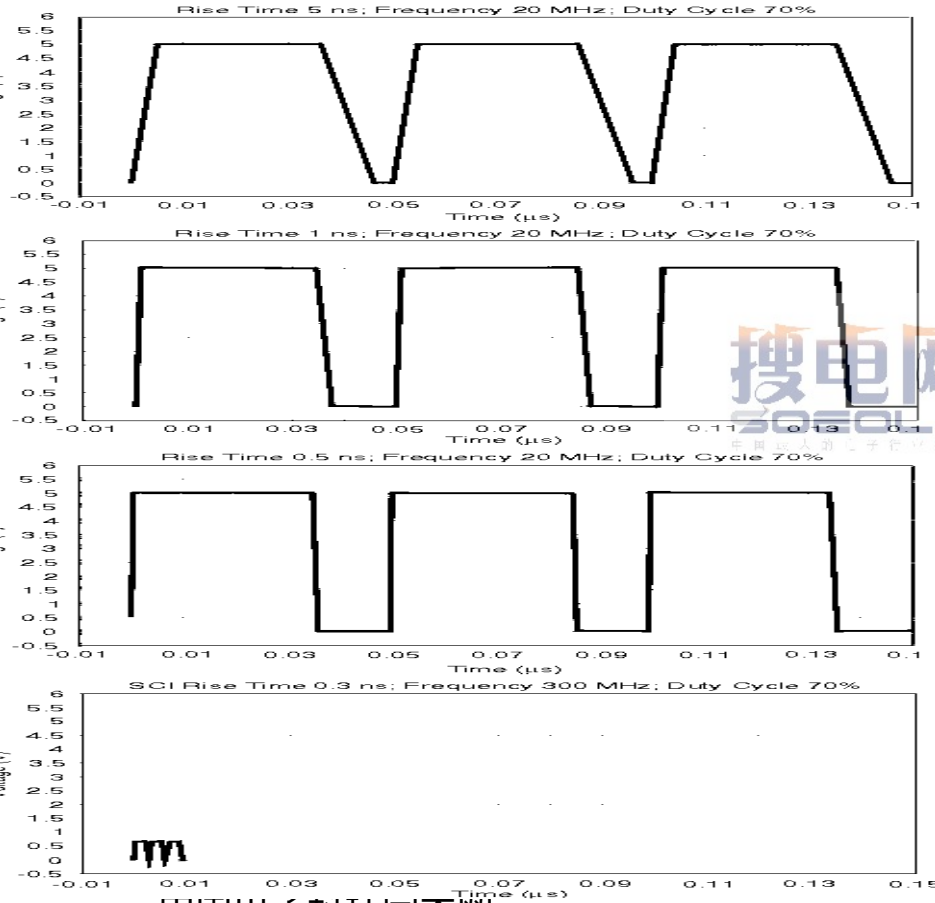
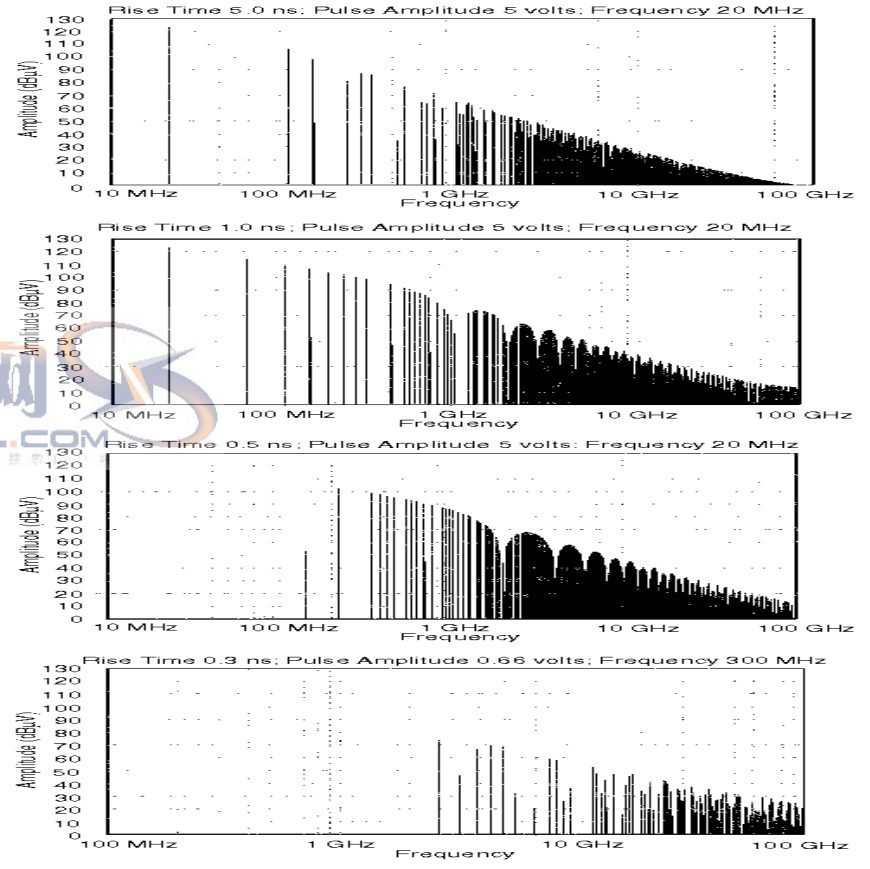
PCB的电磁兼容设计

脉冲信号的频谱

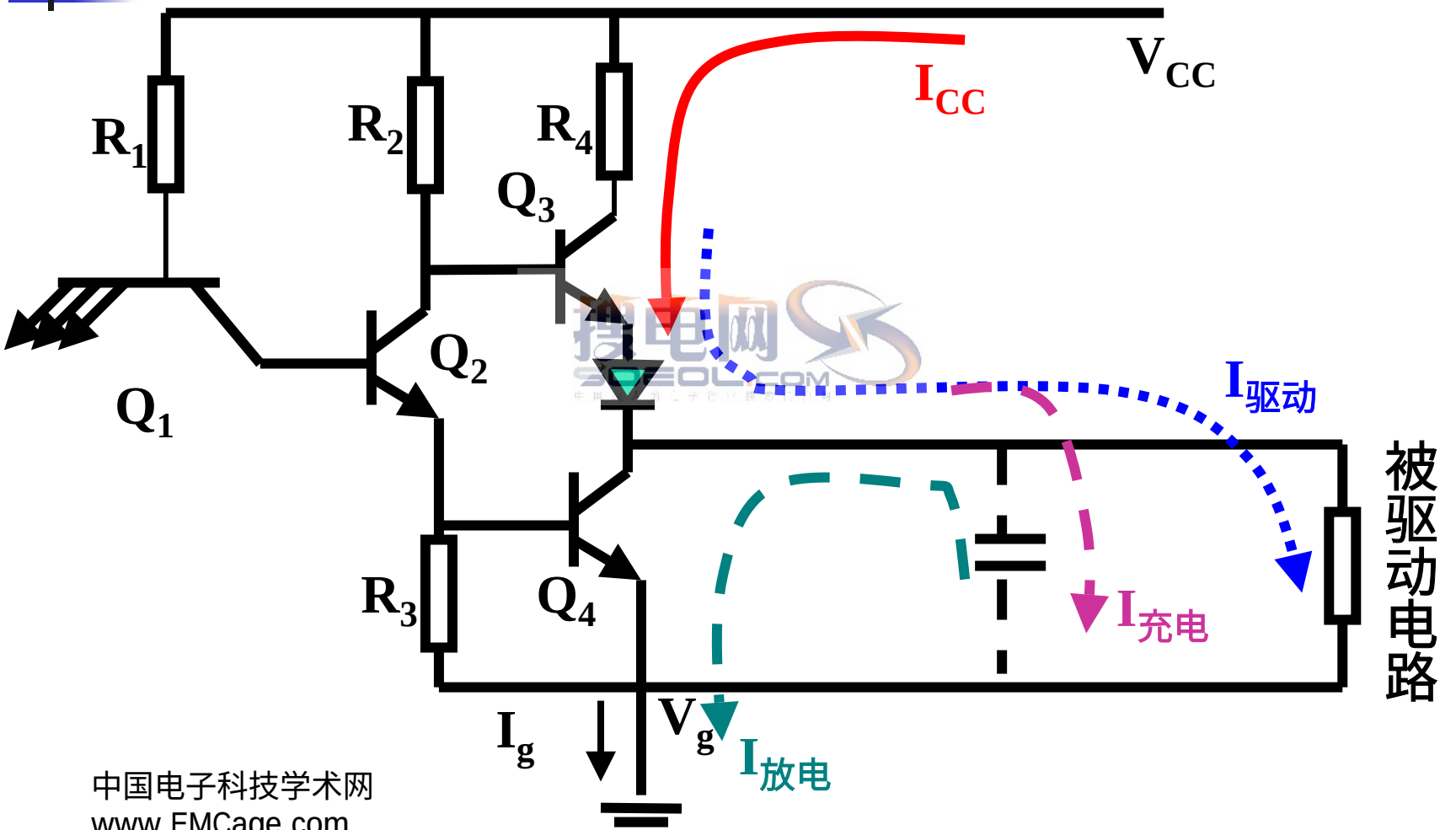


上升沿越陡高频越丰富

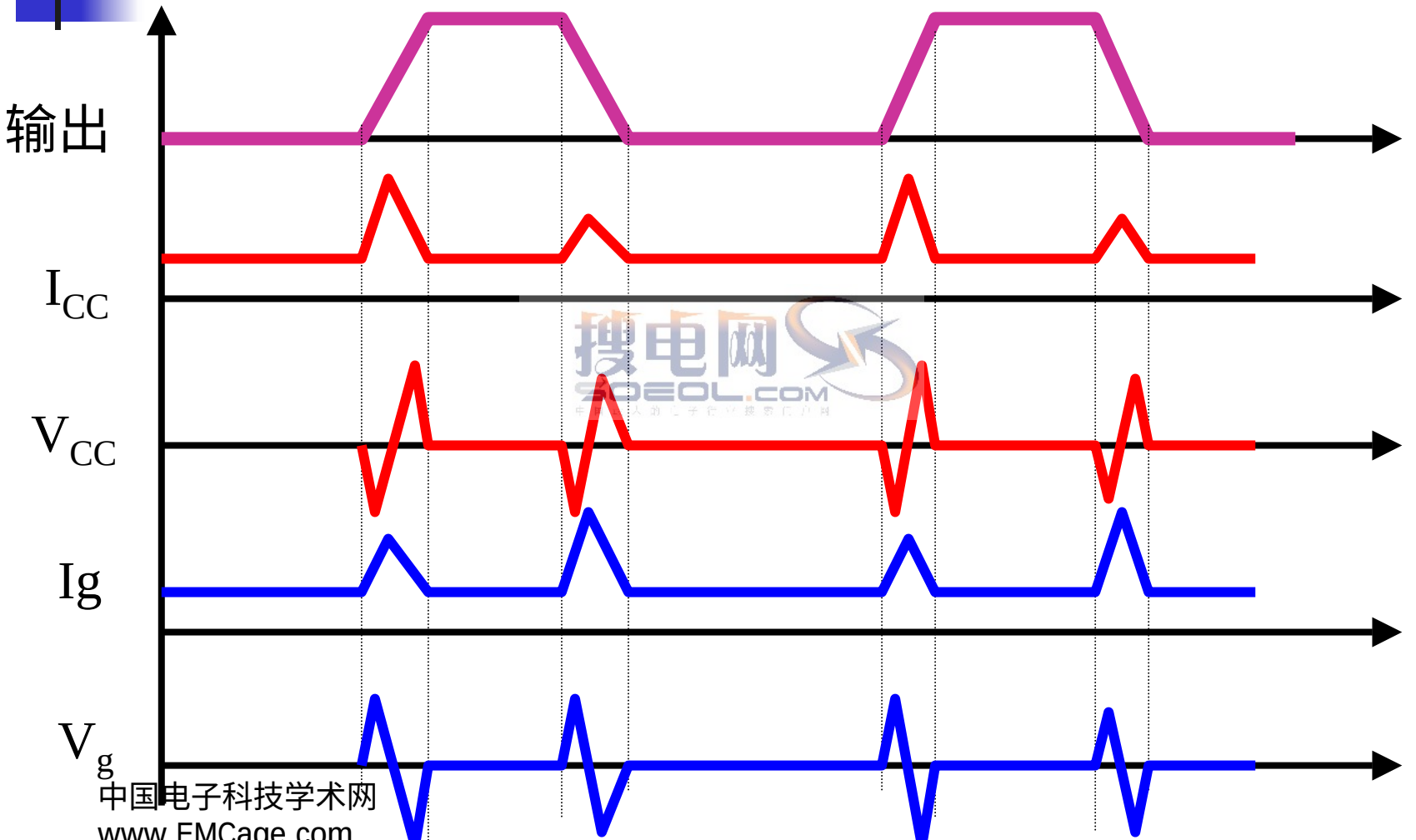




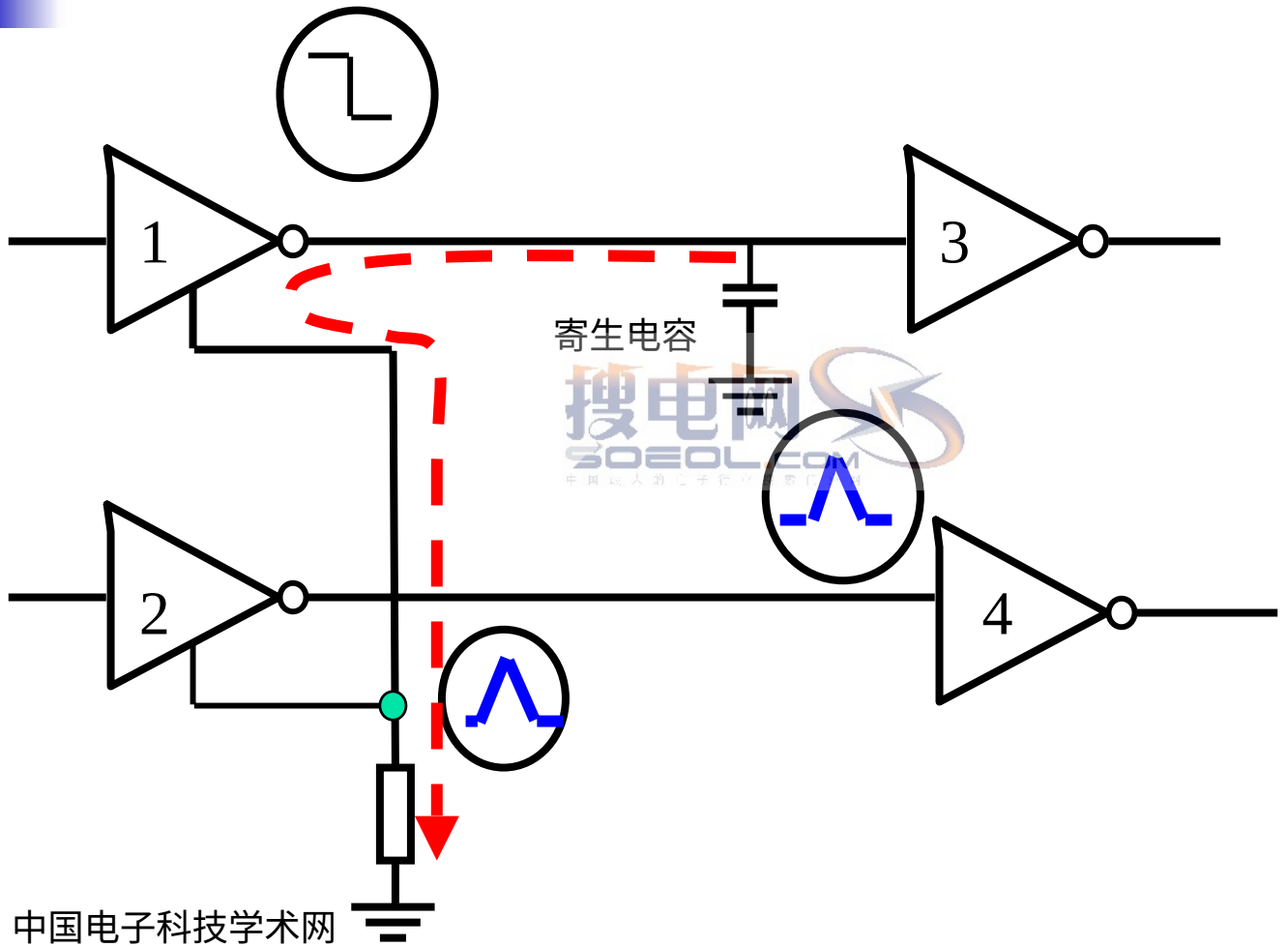
地线和电源线上的噪声



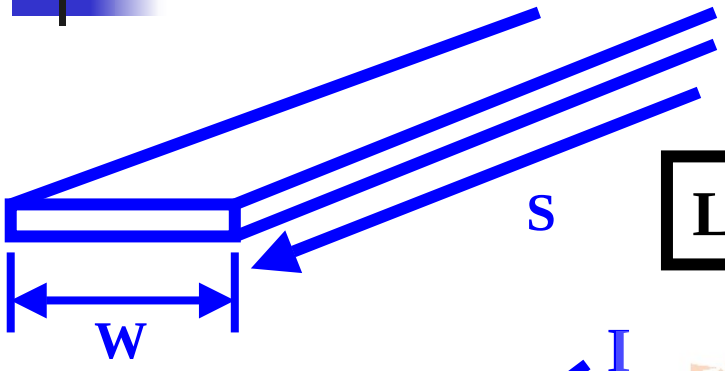
电源线、地线噪声电压波形



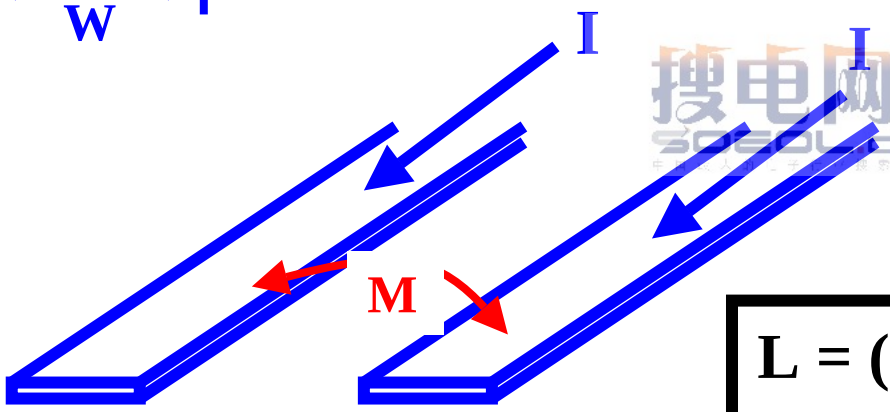
地线干扰对电路的影响



线路板走线的电感



$$L = 0.002S(2.3\lg(2S/W) + 0.5 \quad \mu H$$

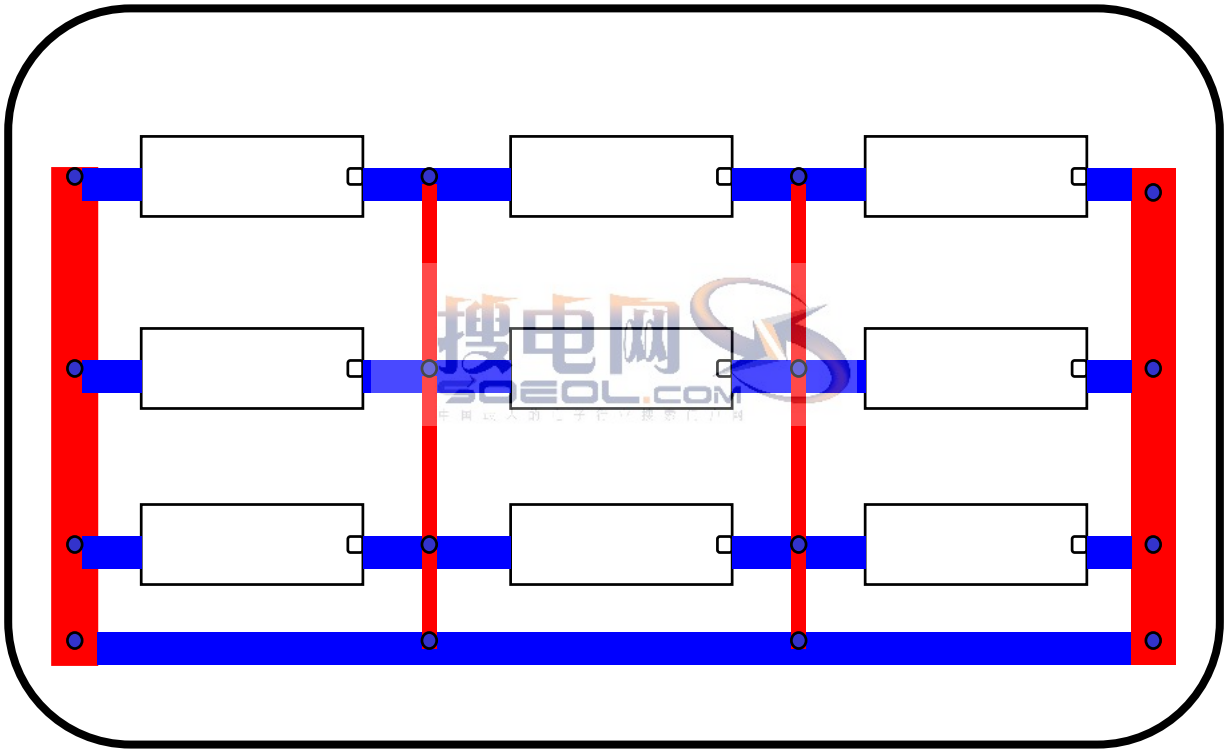


$$L = (L_1L_2 - M^2) / (L_1 + L_2 - 2M)$$

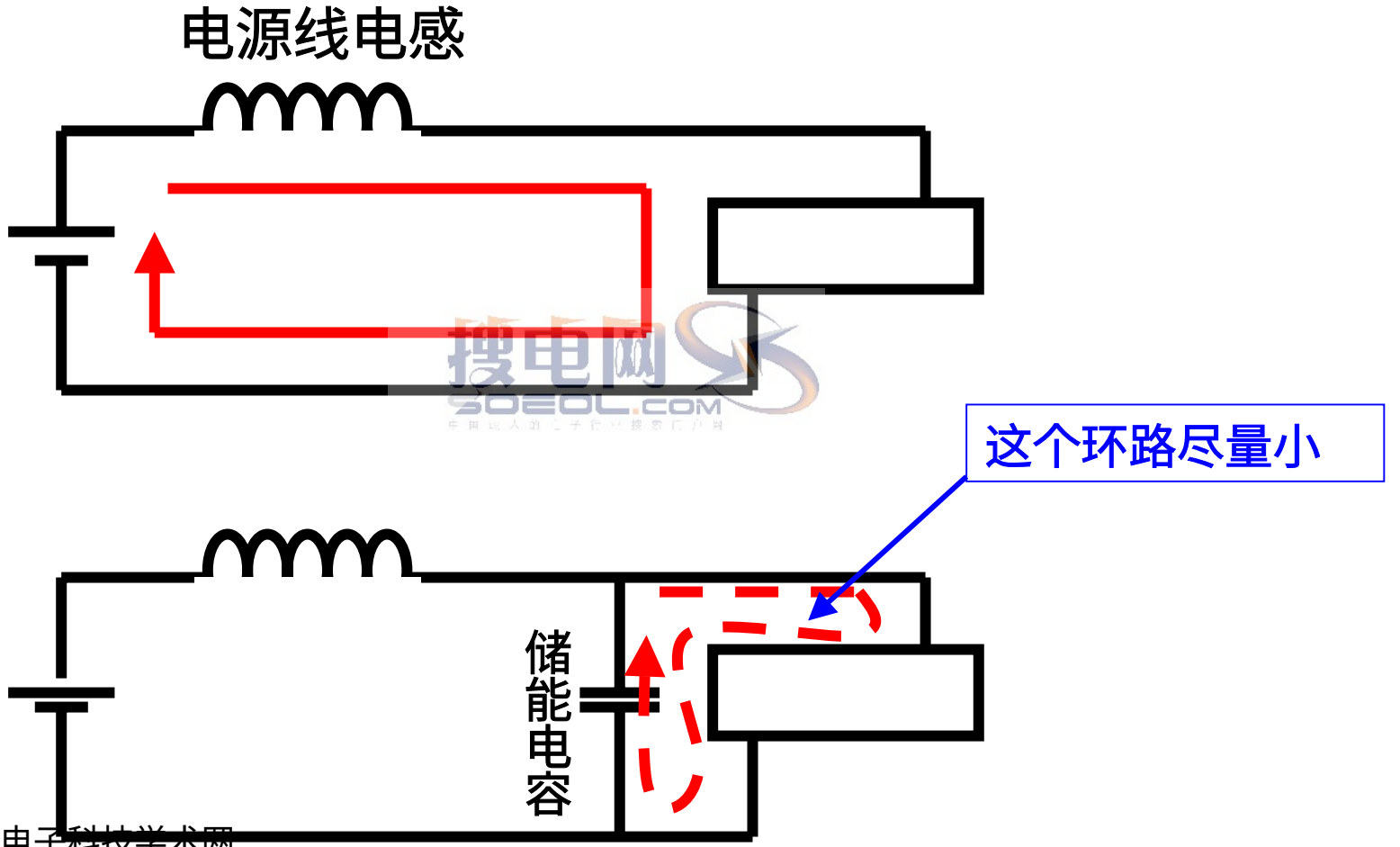
若：$L_1 = L_2$

$$L = (L_1 + M) / 2$$

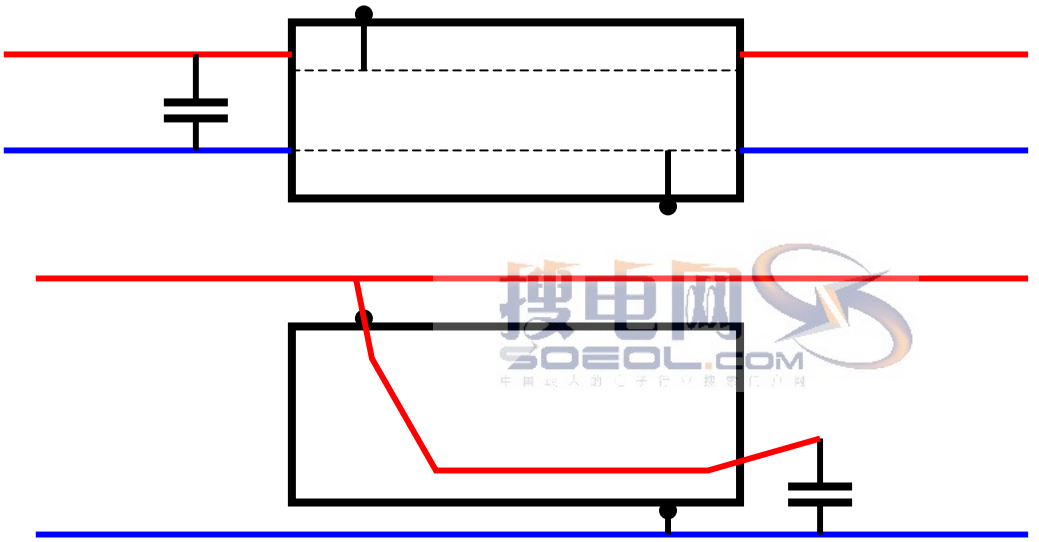
地线网格



电源线噪声的消除



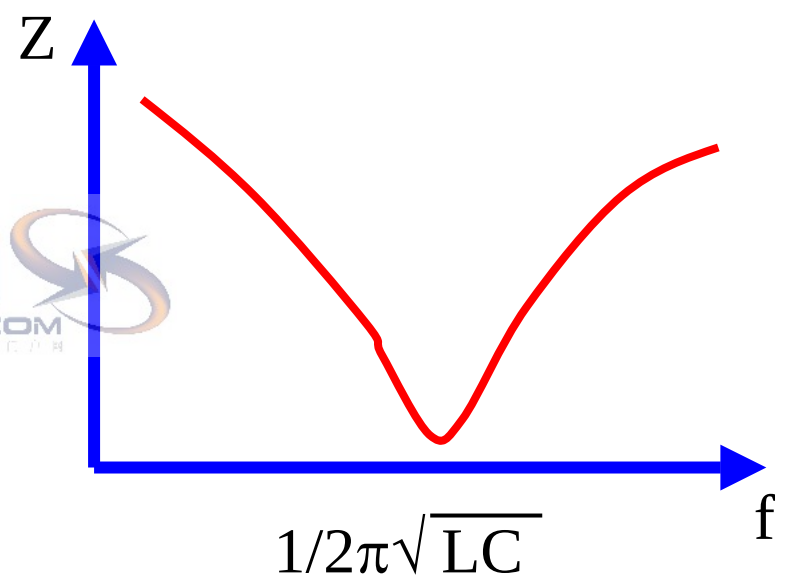
电源解耦电容的正确布置



尽量使电源线与地线靠近

解耦电容的选择

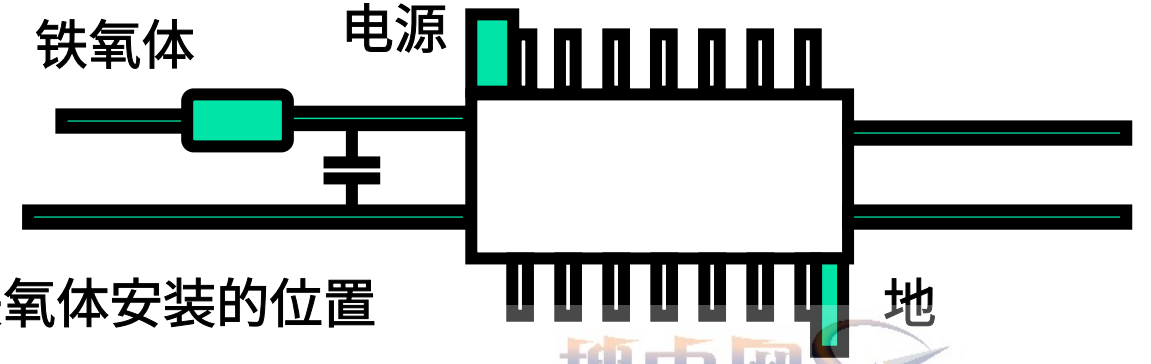
$$C = \frac{dI\ dt}{dV}$$



各参数含义：

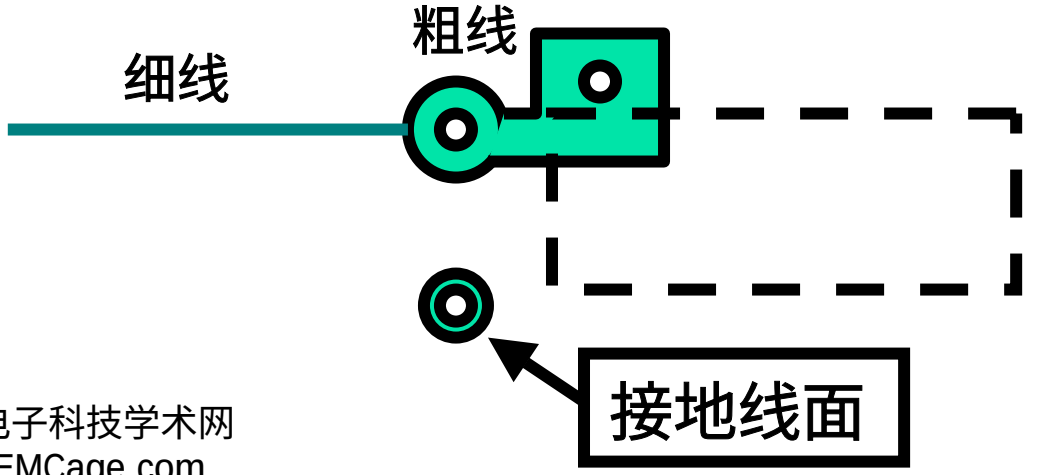
在时间dt内，电源线上出现了瞬间电流dI，dI导致了电源线上出现电压跌落dV。

增强解耦效果的方法



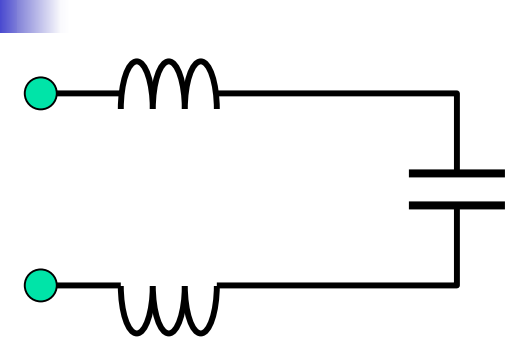
用铁氧体增加电源端阻抗

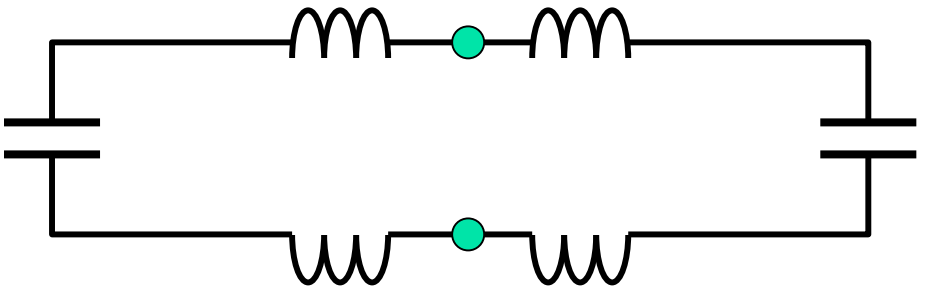
注意铁氧体安装的位置

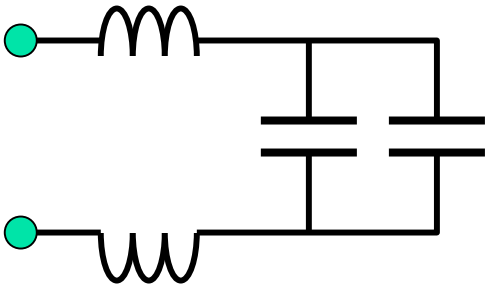


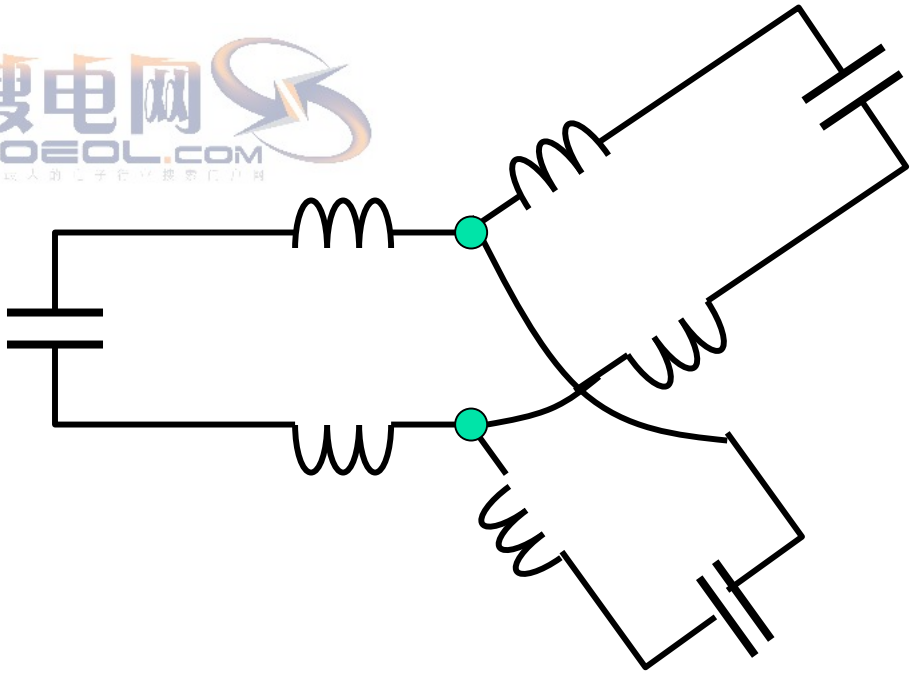
用细线增加电源端阻抗

多个电容并联加强解耦效果

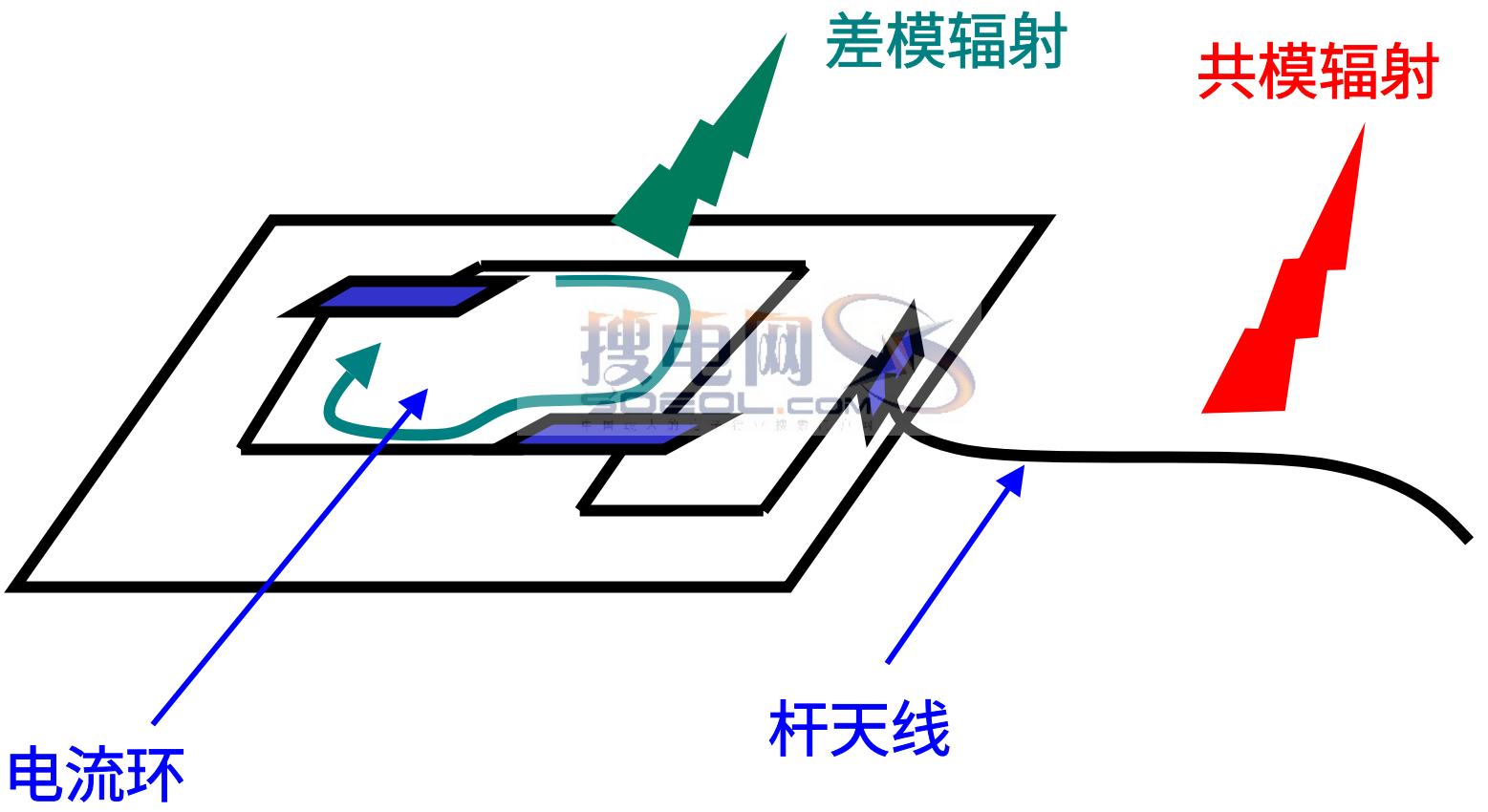








线路板的两种辐射机理



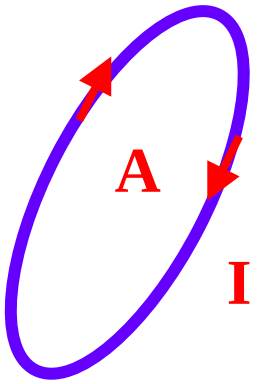
电流环路产生的辐射

近场区内：

$H = IA / (4\pi D^3)$ A/m

$E = Z_0 IA / (2\lambda D^2)$ V/m

$Z_W = Z_0 (2\pi D/\lambda)$ Ω



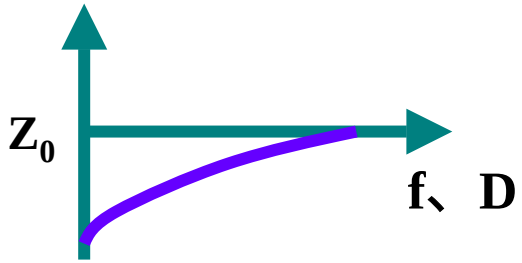
随频率、距离增加而增加

远场区内：

$H = \pi IA / (\lambda^2 D)$ A/m

$E = Z_0 \pi IA / (\lambda^2 D)$ V/m

$Z_W = Z_0 = 377$ Ω

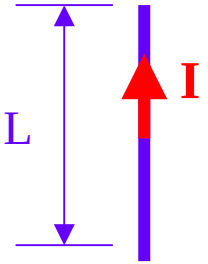


导线的辐射

近场区内：　$H = I L / (4\pi D^2)$　　A/m

$E = Z_0 I L \lambda / (8 \pi^2 D^3)$　　V/m

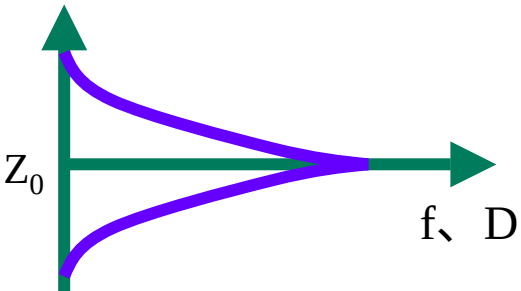
$Z_W = Z_0 (\lambda/2\pi D)$　　Ω



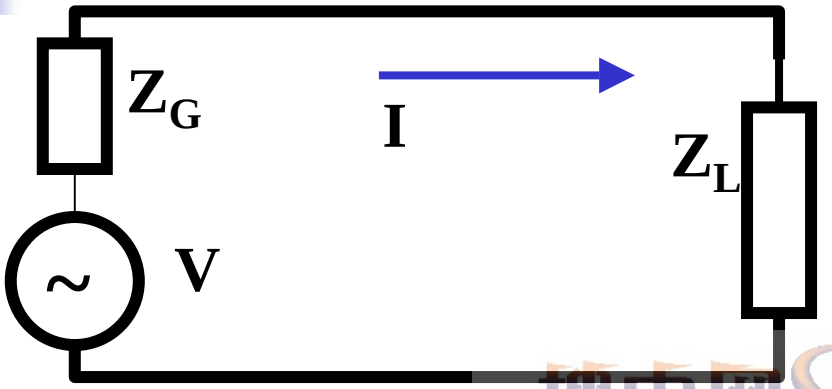
远场区内：　$H = I L / (2\lambda D)$　　A/m

$E = Z_0 I L / (2\lambda D)$　　V/m

随频率、距离增加而减小



实际电路的辐射



$Z_C = Z_G + Z_L$

环路面积 = A

近场：$Z_C \geq 7.9\ D\ f$　　$E = 7.96VA / D^3$　　（μV/m）

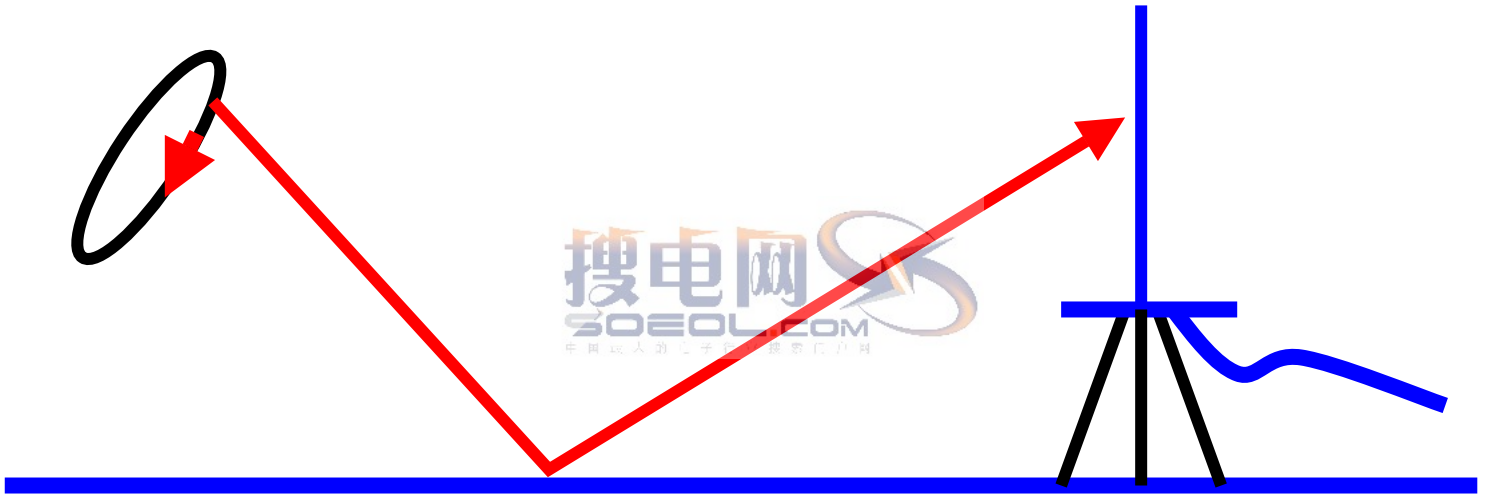
$Z_C \leq 7.9\ D\ f$，　$E = 63\ I\ A\ f / D^2$　　（μV/m）

$H = 7.96IA / D^3$　　（μA/m）

远场：

$E = 1.3\ I\ A\ f^2 / D$　　（μV/m）

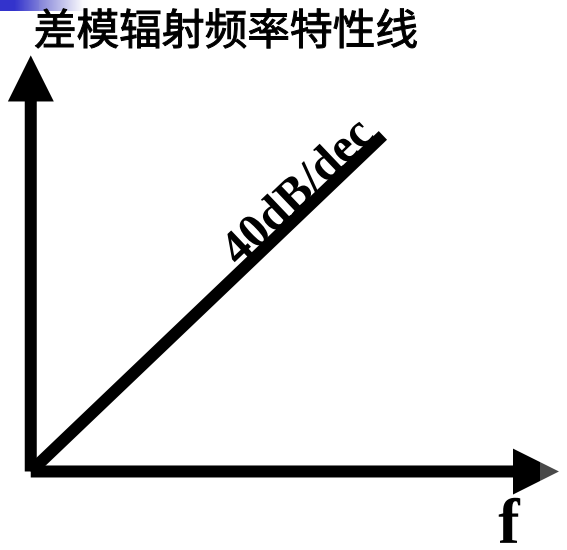
常用的差模辐射预测公式

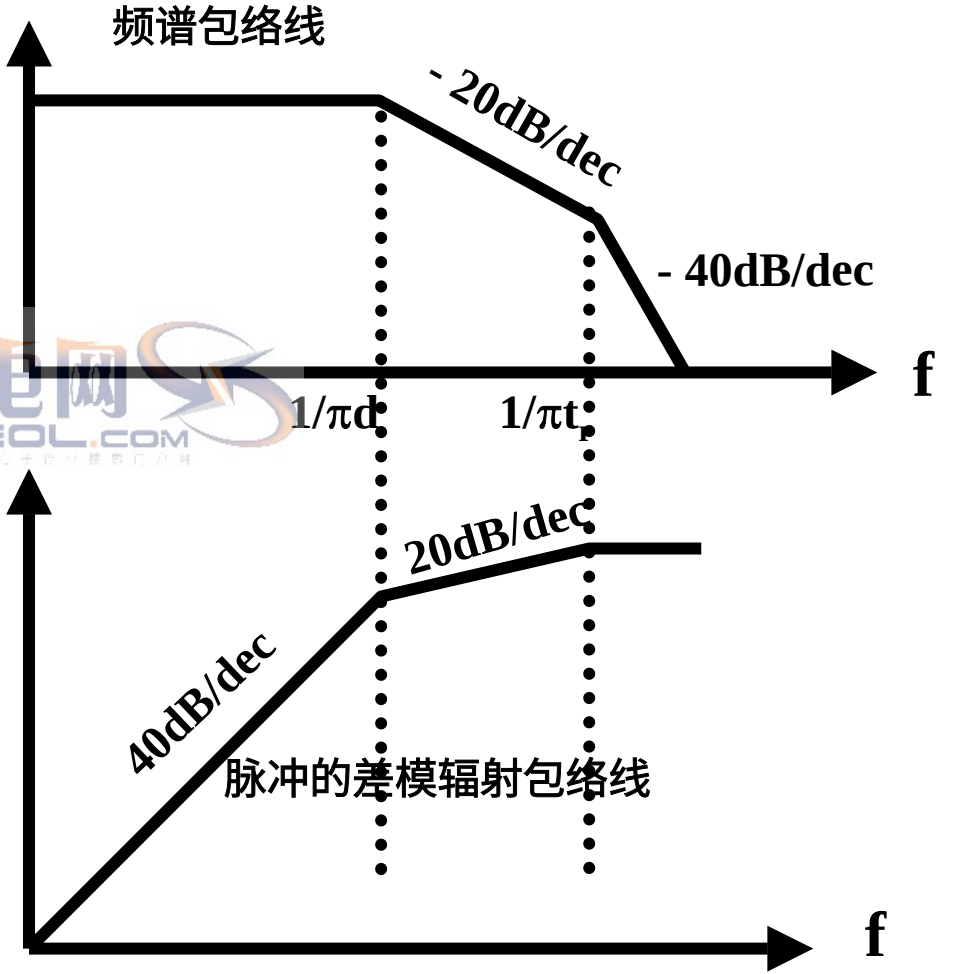


考虑地面反射时：

$$E = 2.6\ I\ A\ f^{2}/D \qquad (\mu V/m)$$

脉冲信号差模辐射的频谱





$$E = 2.6\ I\ A\ f^2/D$$

$$E_{dB} = 20\lg(2.6\ I\ A/D) + 40\lg f$$

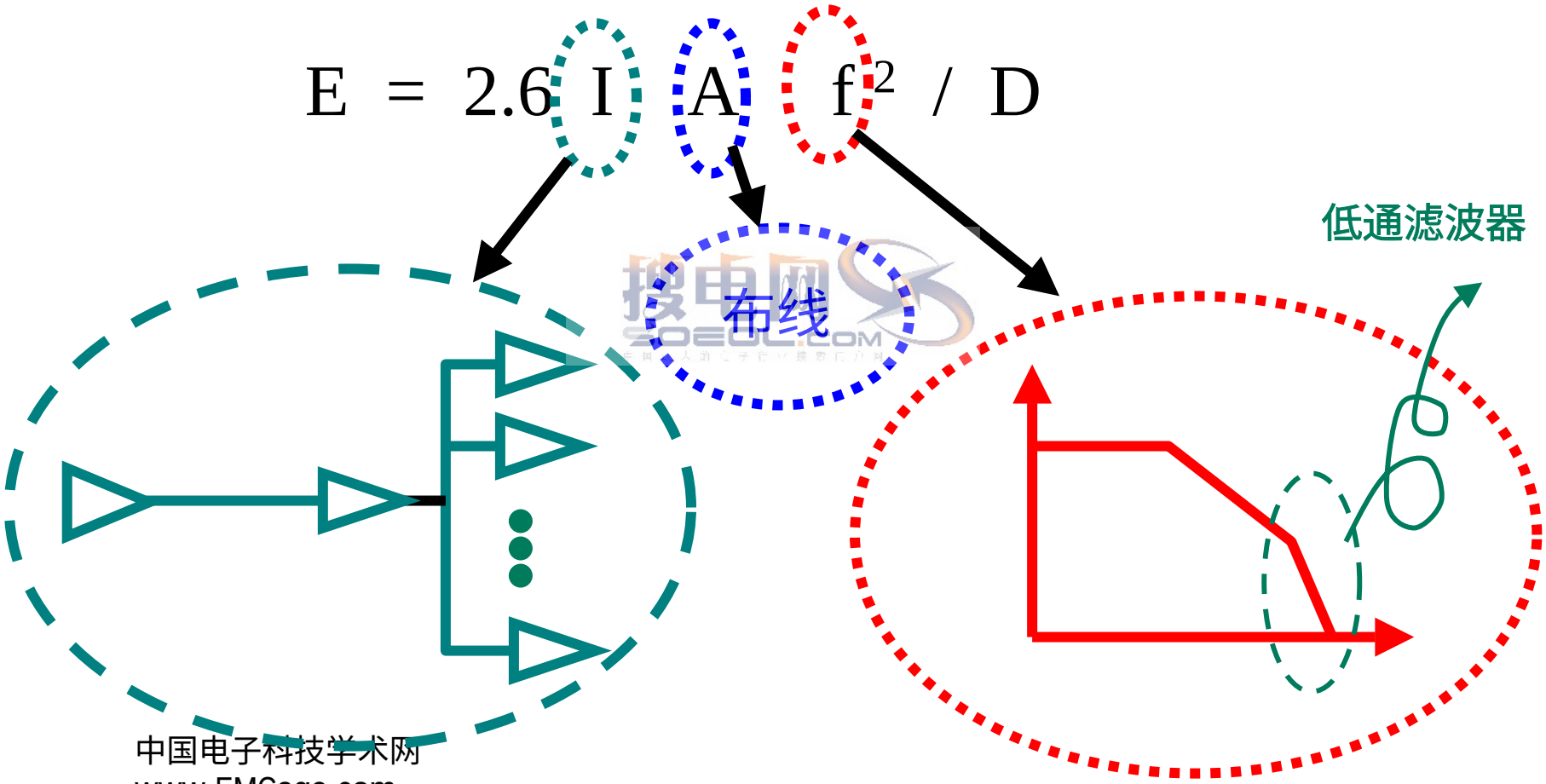
不同逻辑电路为了满足EMI指标要求所允许的环路面积

逻辑系列	上升时间	电流	不同时钟频率允许的面积（cm^2）			
			4MHz	10	30	100
4000B	40	6	1000	400		
74HC	6	20	50	45	18	6
74LS	6	50	20	18	7.2	2.4
74AC	3.5	80	5.5	2.2	0.75	0.25
74F	3	80	5.5	2.2	0.75	0.25
74AS	1.4	120	2	0.8	3	0.15

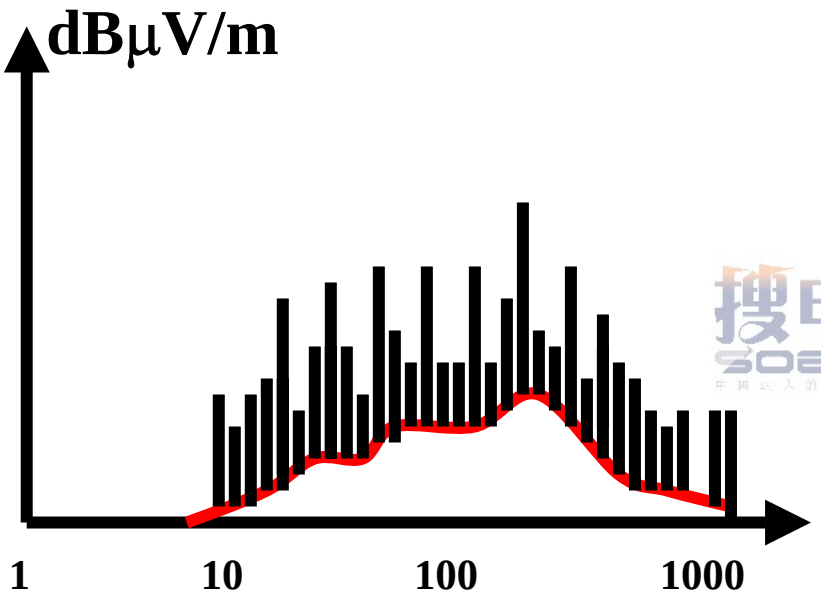
仅代表了一个环路的辐射情况，若有N个环路辐射，乘以$\sqrt{N}$。因此，可能时，分散时钟频率。

如何减小差模辐射？

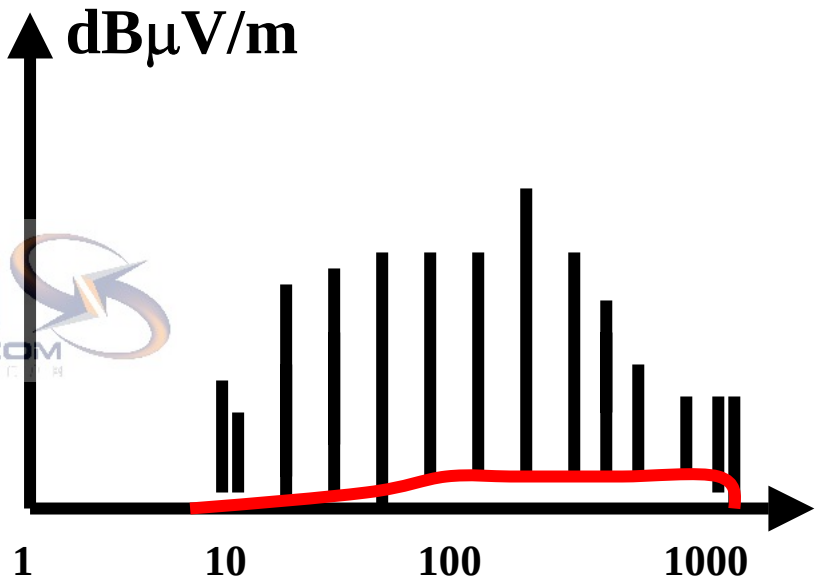
$$E = 2.6\ I\ A\ f^2\ /\ D$$



电路中的强辐射信号

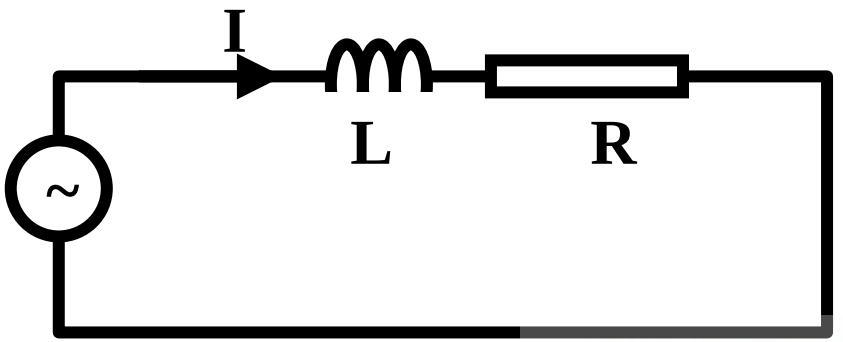


所有电路加电工作



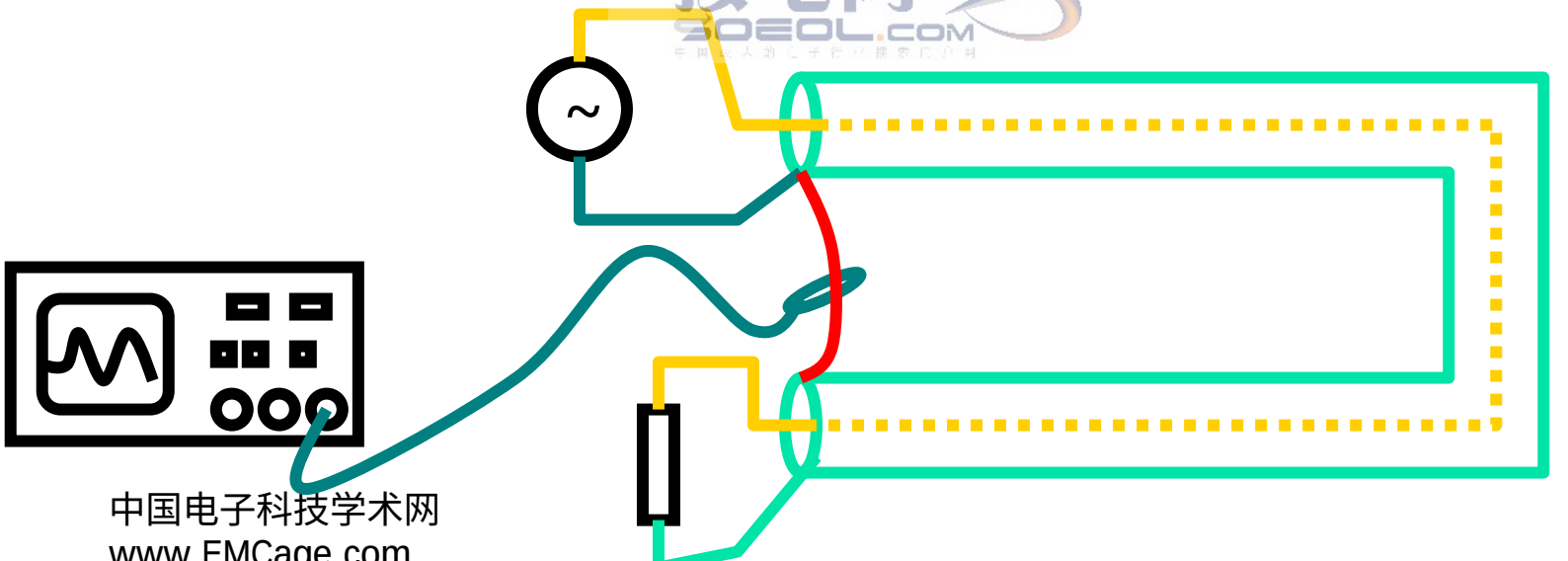
只有时钟电路加电工作

电流回路的阻抗

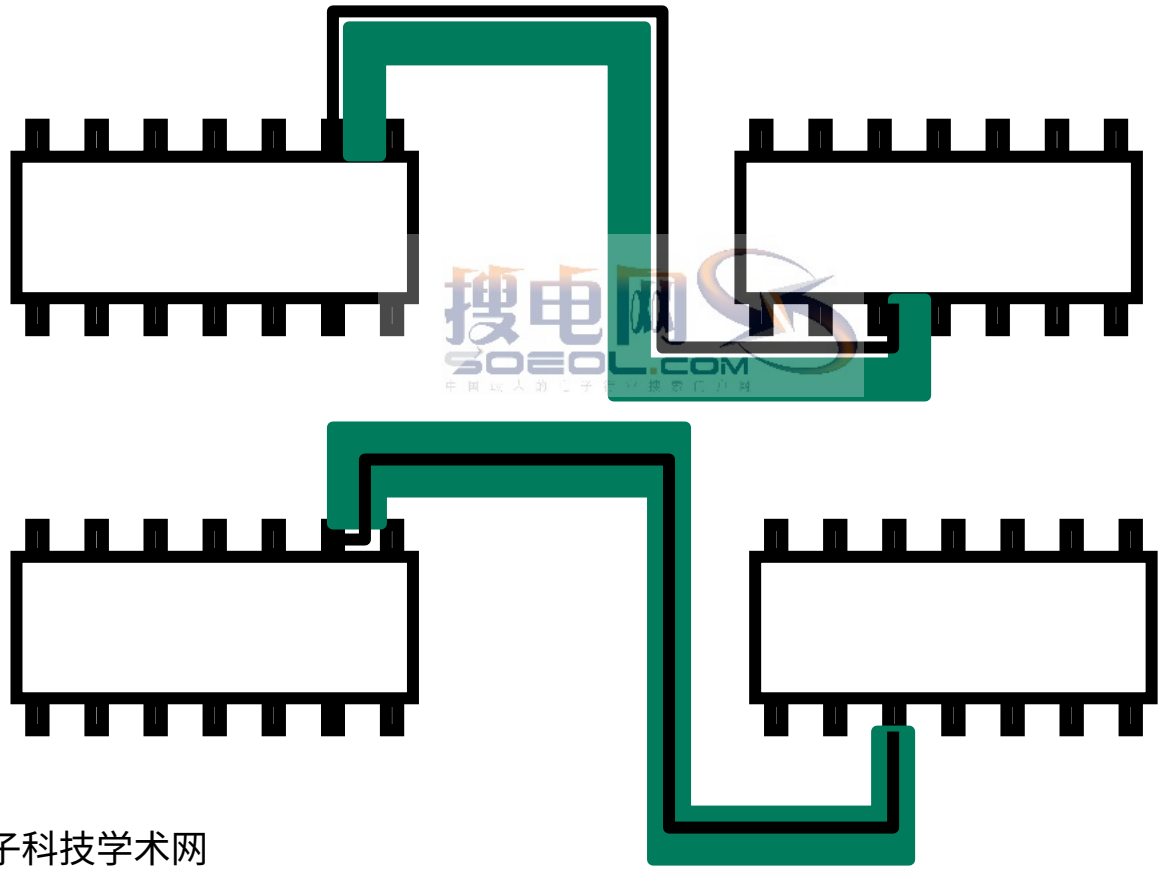


$$Z = R + j\omega L$$

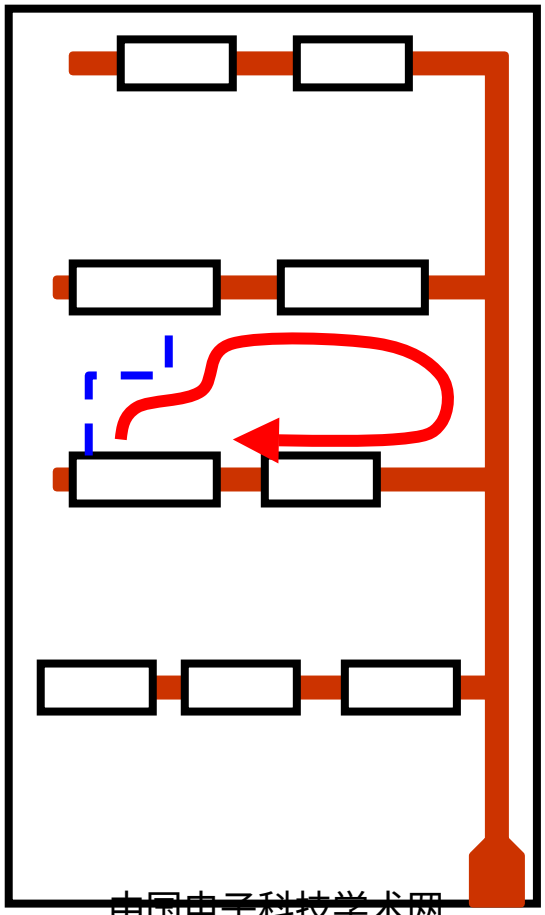
$$L = \Phi / I \qquad \Phi \propto A$$

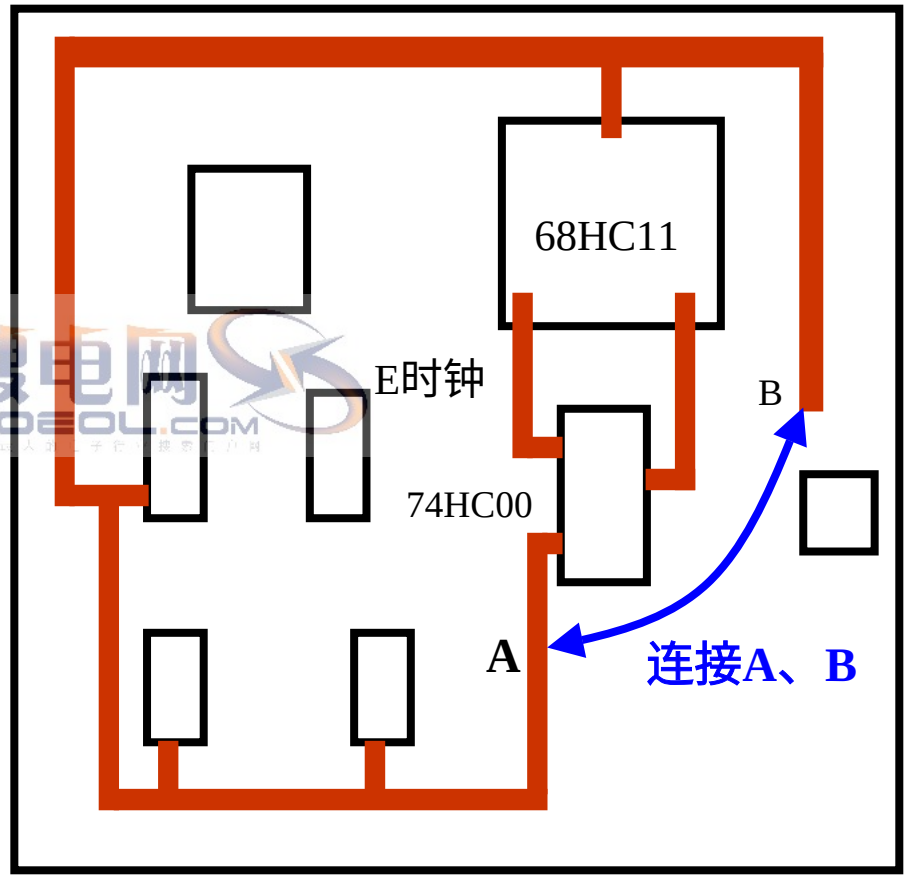


单层或双层板如何减小环路的面积

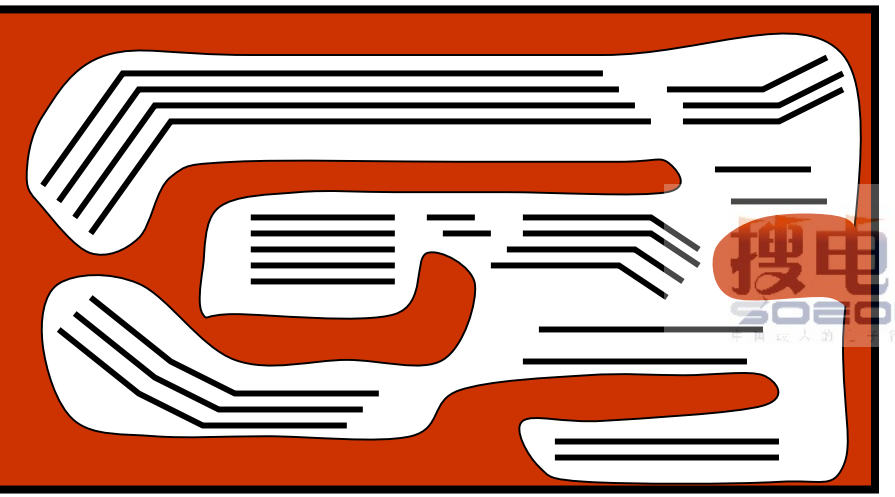


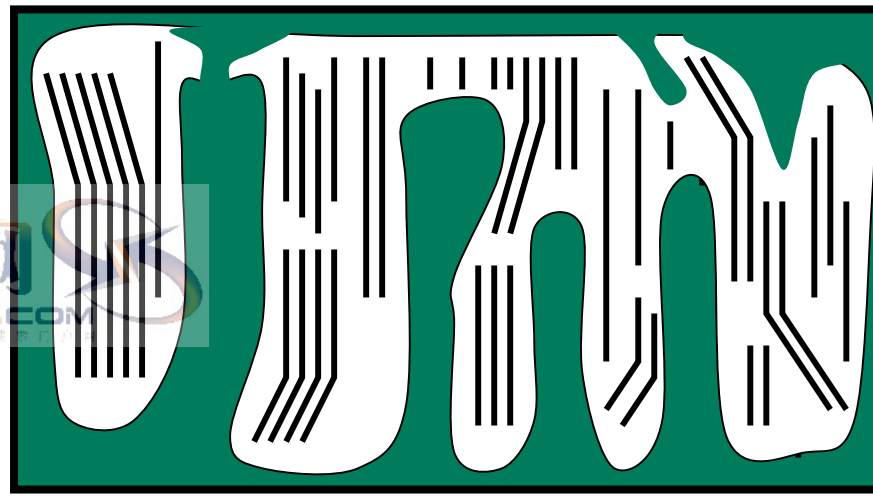
不良布线举例



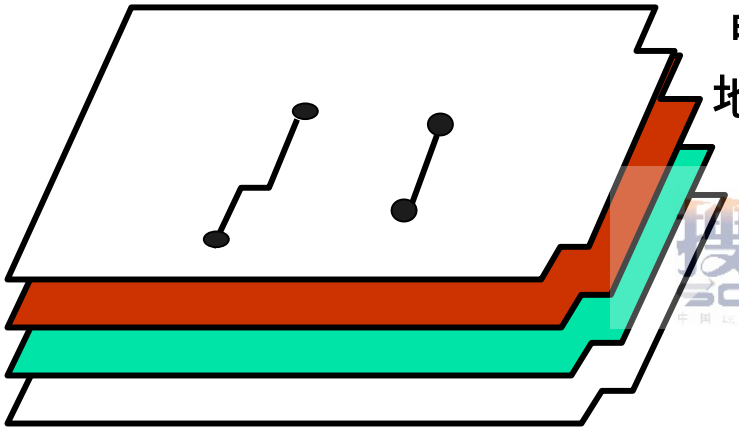


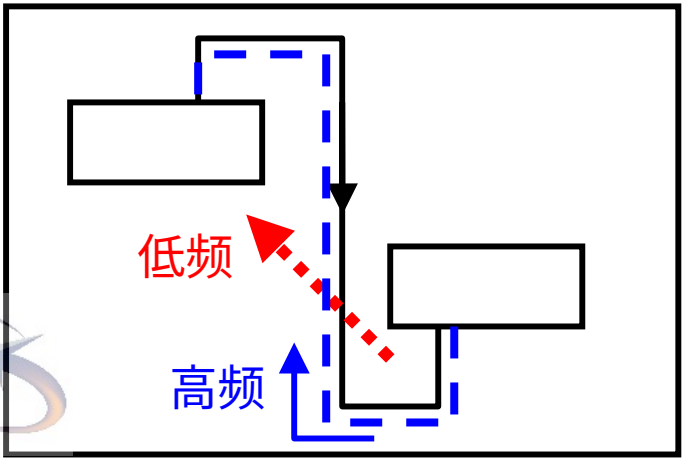
随便设置的地线没有用

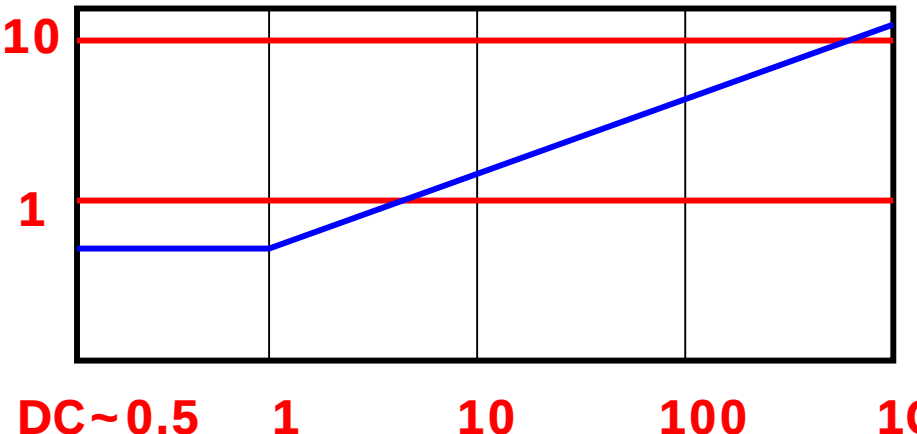




多层板能减小辐射



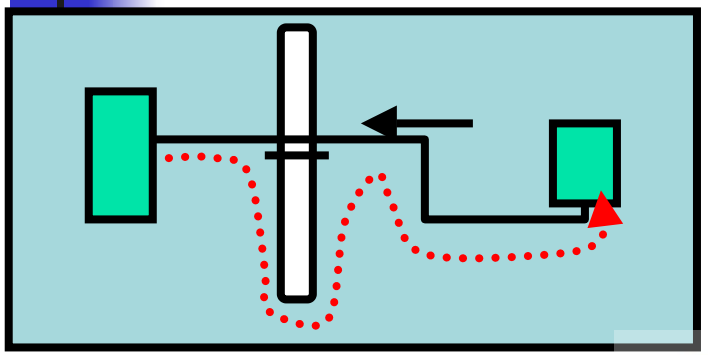


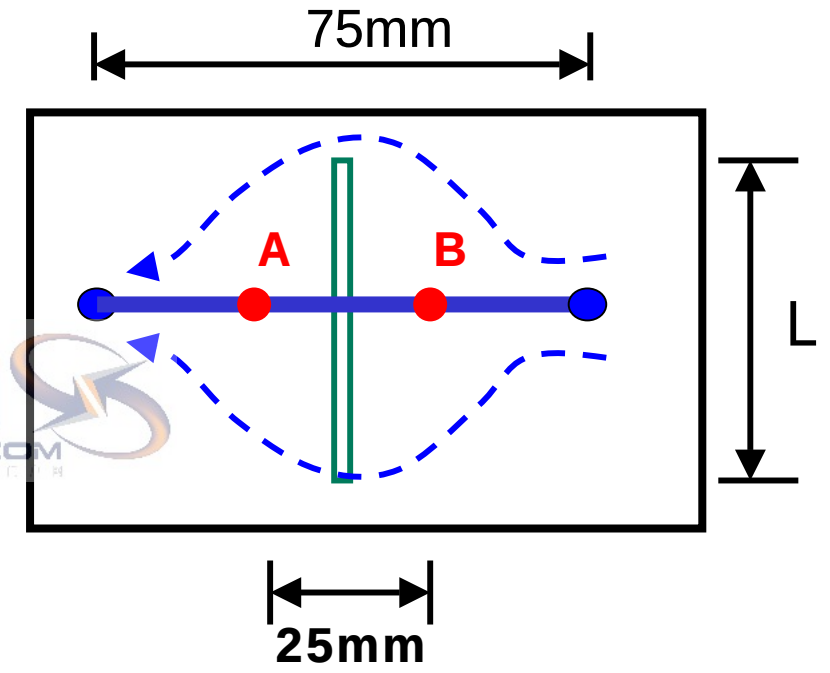


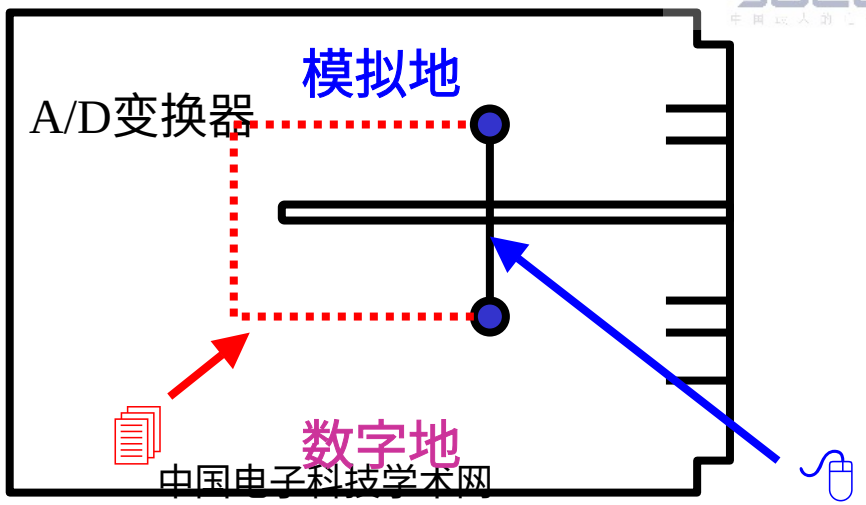
地线面的阻抗，mΩ/ 平方

地线面具有很小的地线阻抗

地线面上的缝隙的影响



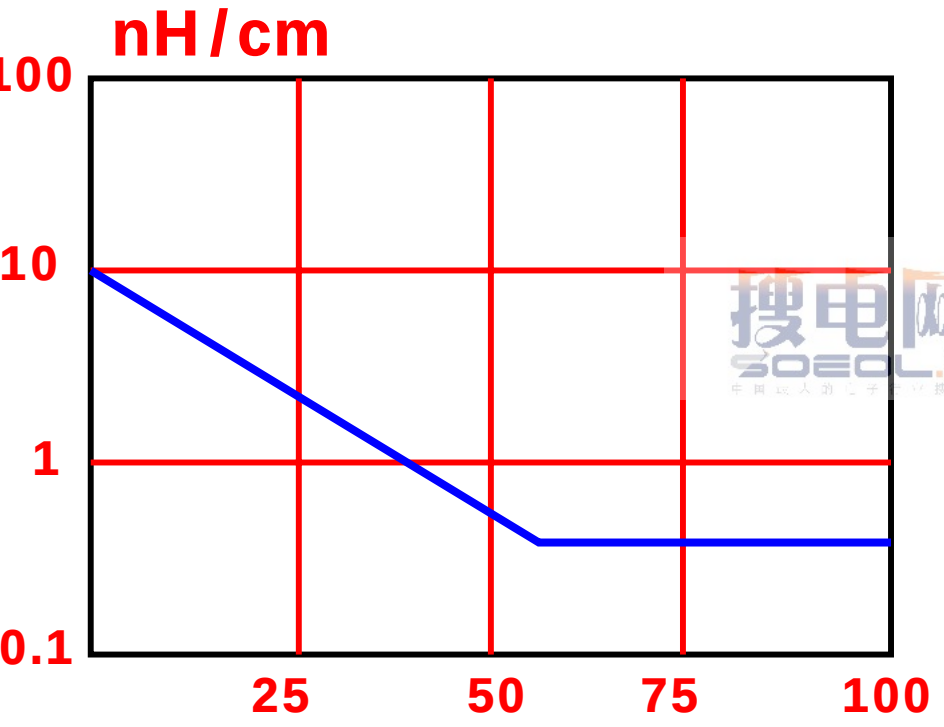


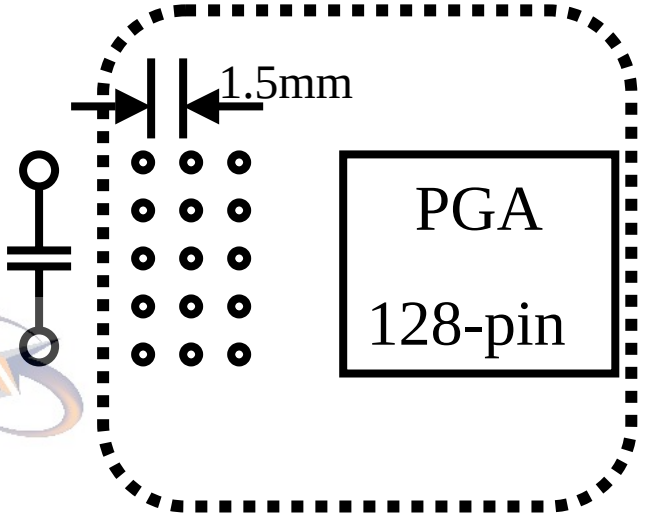


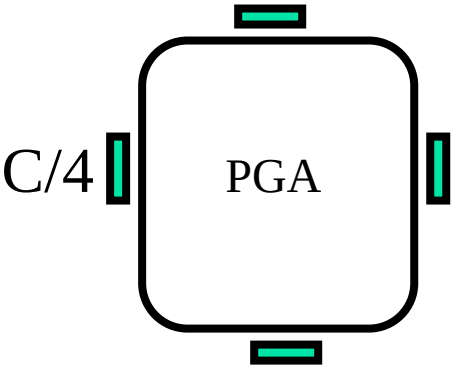
L : 0 ~ 10cm

V_{AB} : 15 ~ 75mV

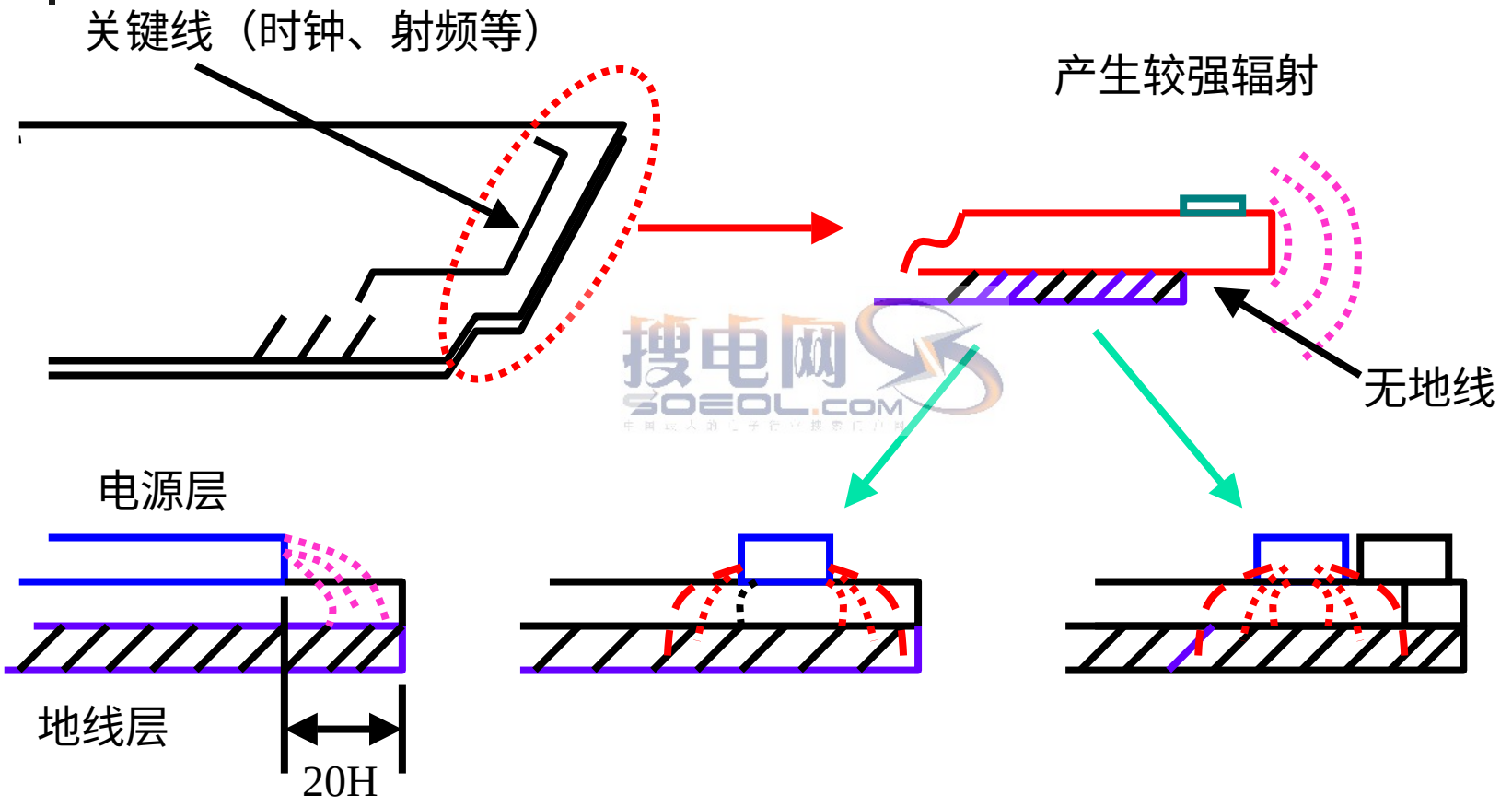
过孔的阻抗





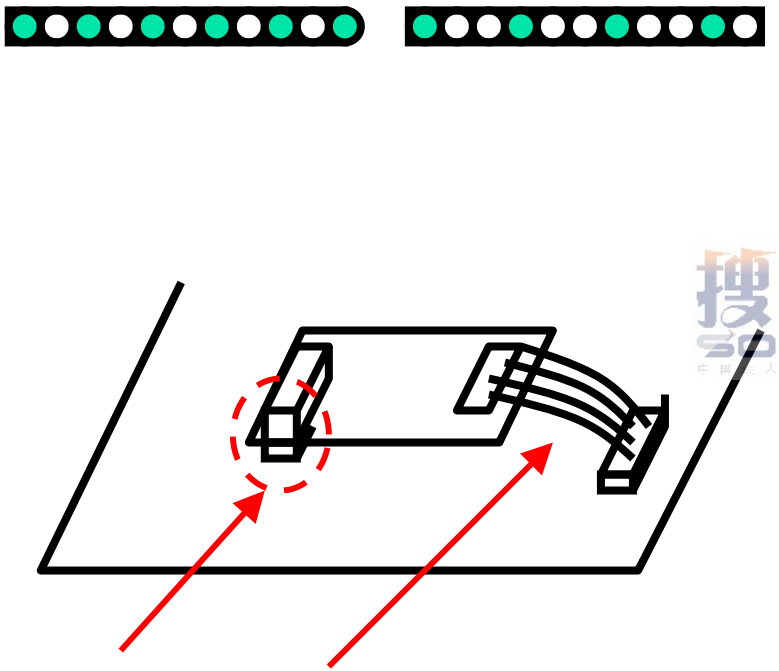


线路板边缘的一些问题

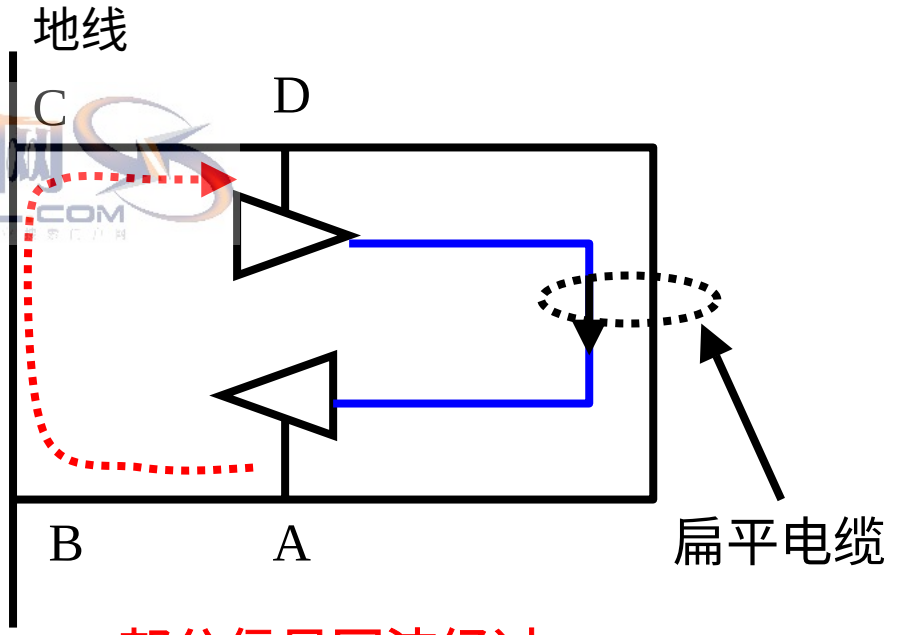


扁平电缆的使用

最好　　较好　　差　　较好，但端接困难

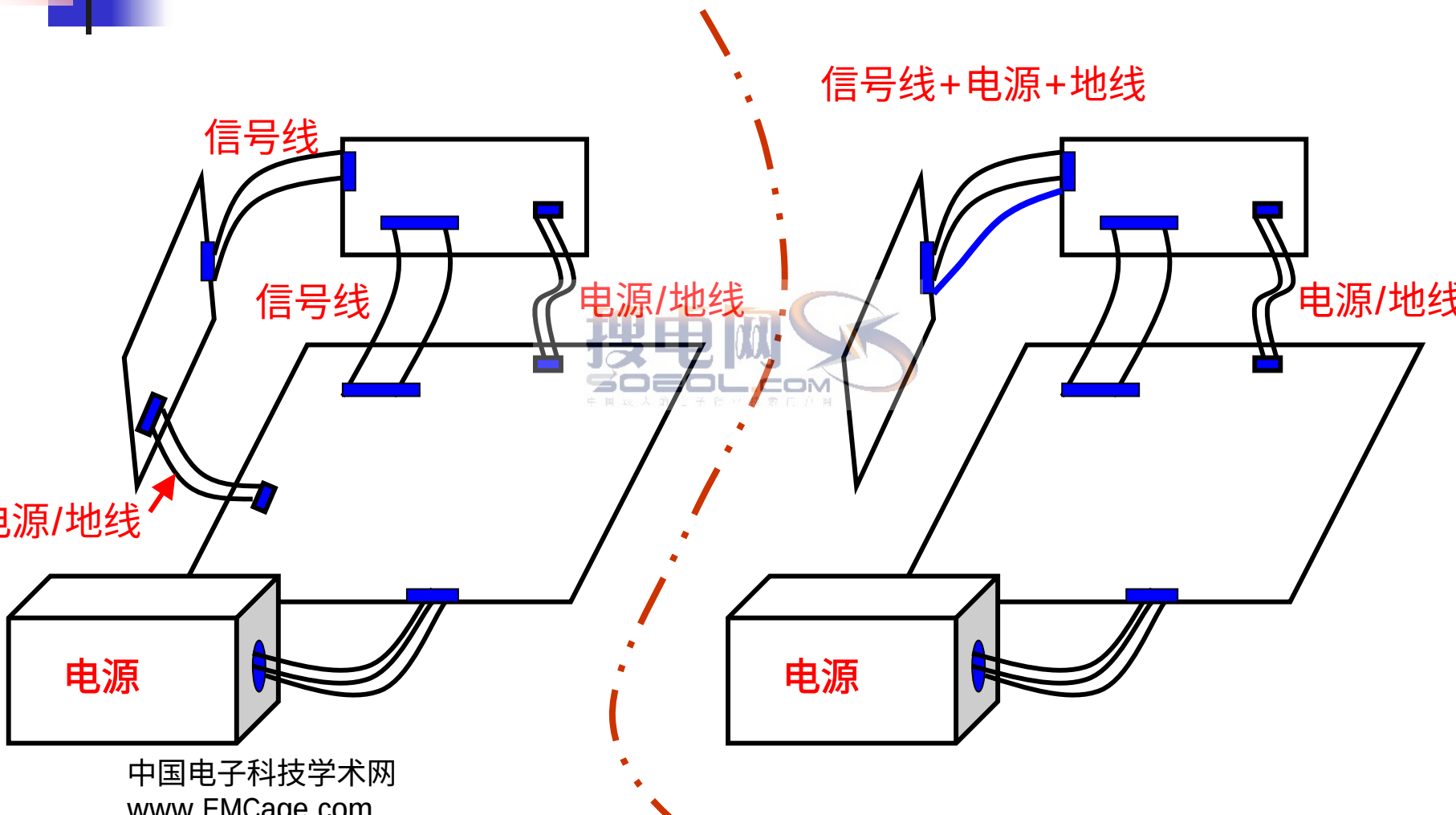


这两处都有地线

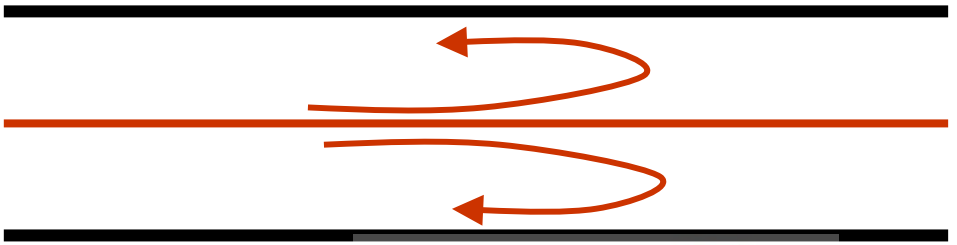


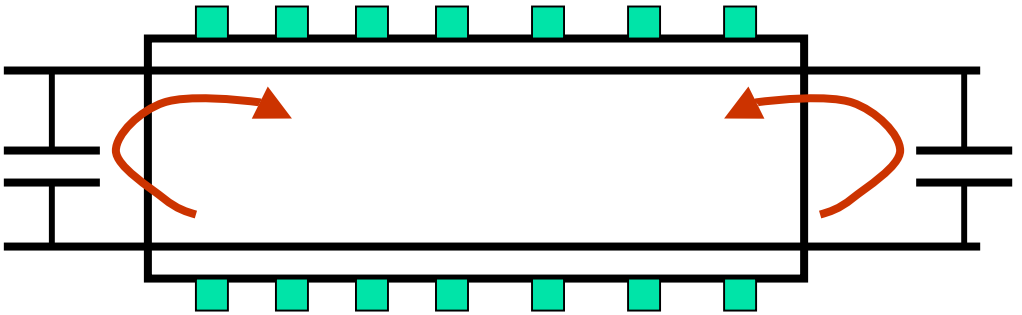
一部分信号回流经过ABCD

注意隐蔽的辐射环路

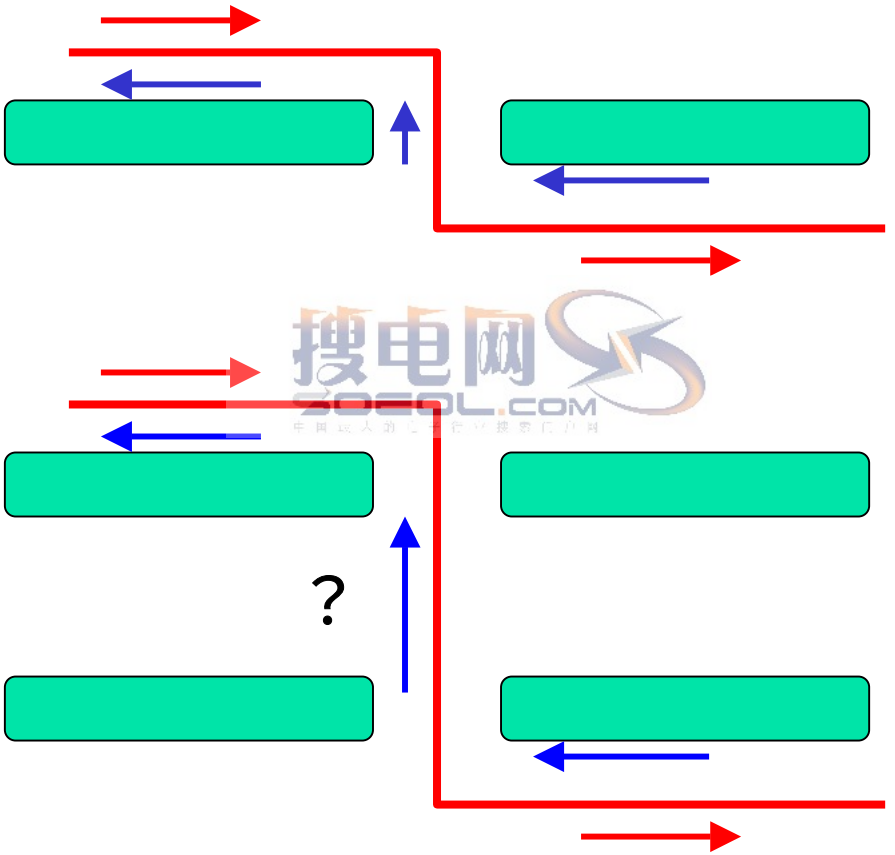


环路对消概念减小辐射

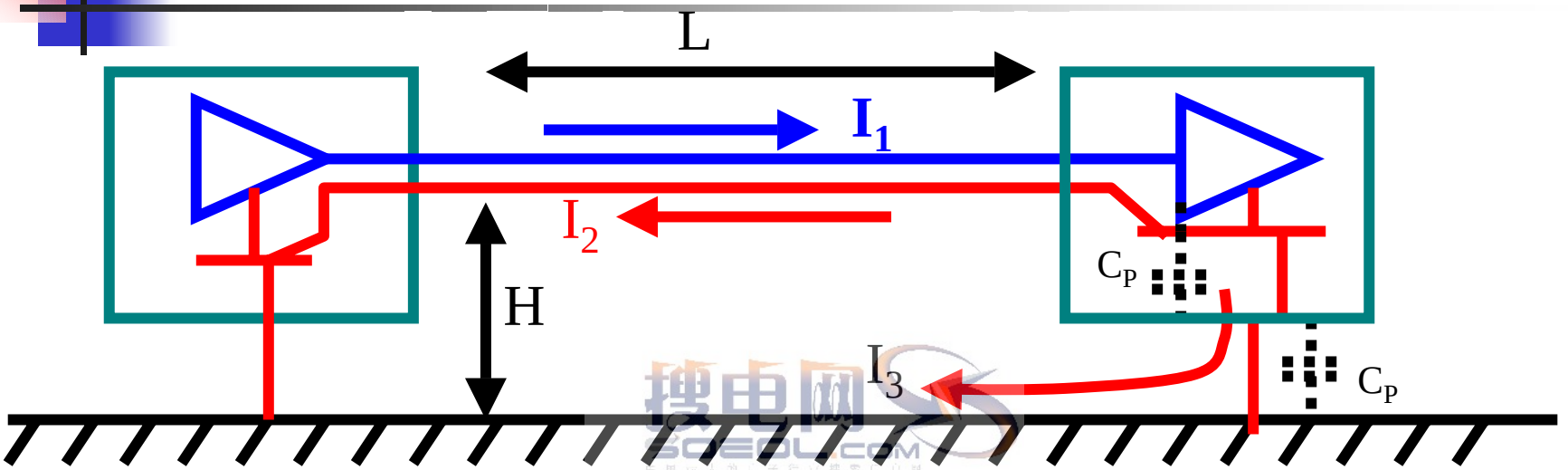


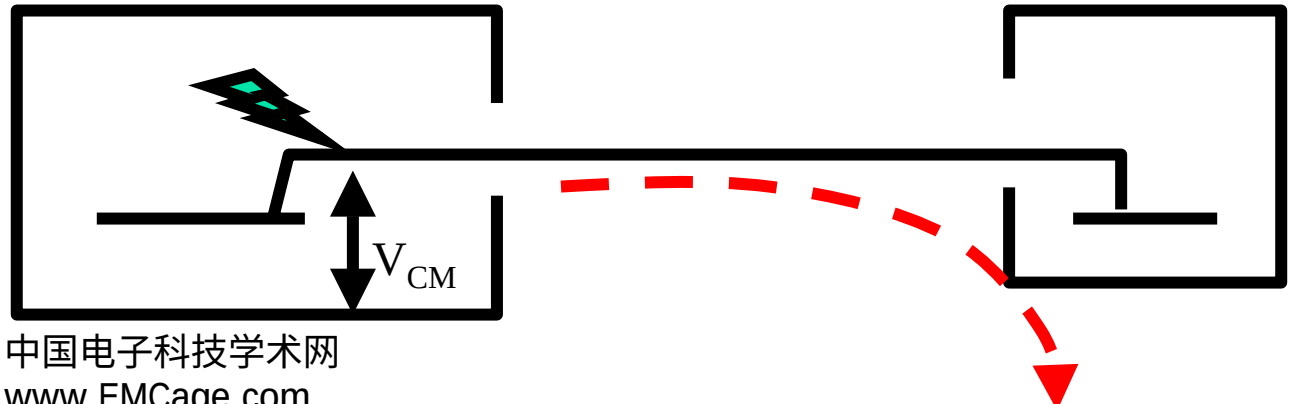


时钟线避免换层



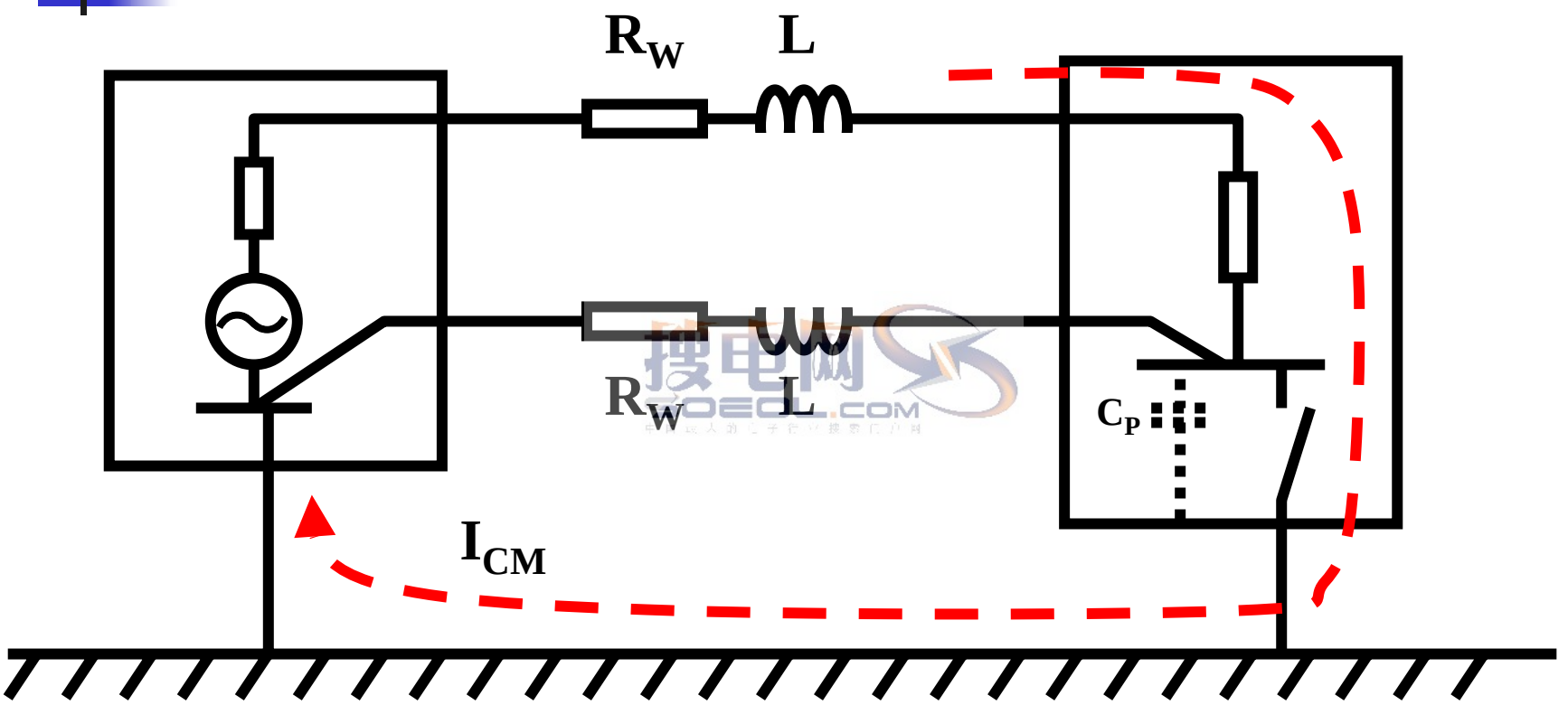
外拖电缆的共模辐射





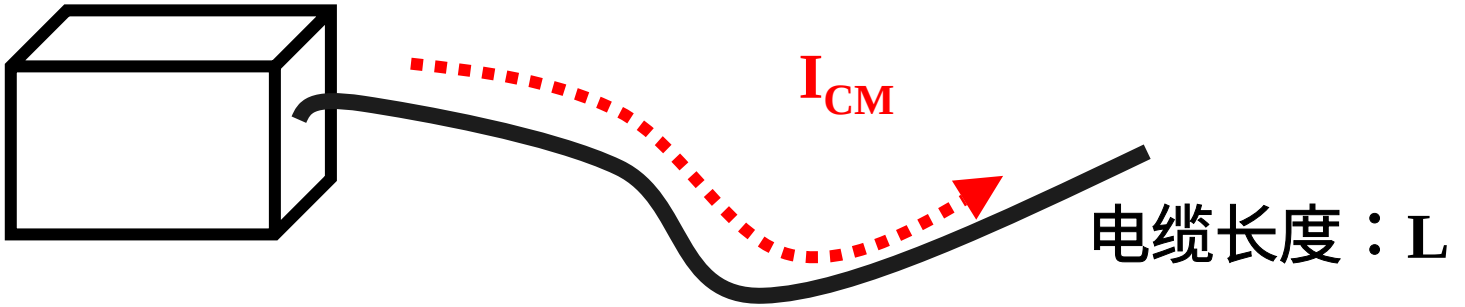
机箱内的所有信号都会通过电缆辐射！

两端设备都接地的情况



$$Z_{CM} = R_W + j\omega L + R_L + 1/ j\omega C$$

悬浮电缆



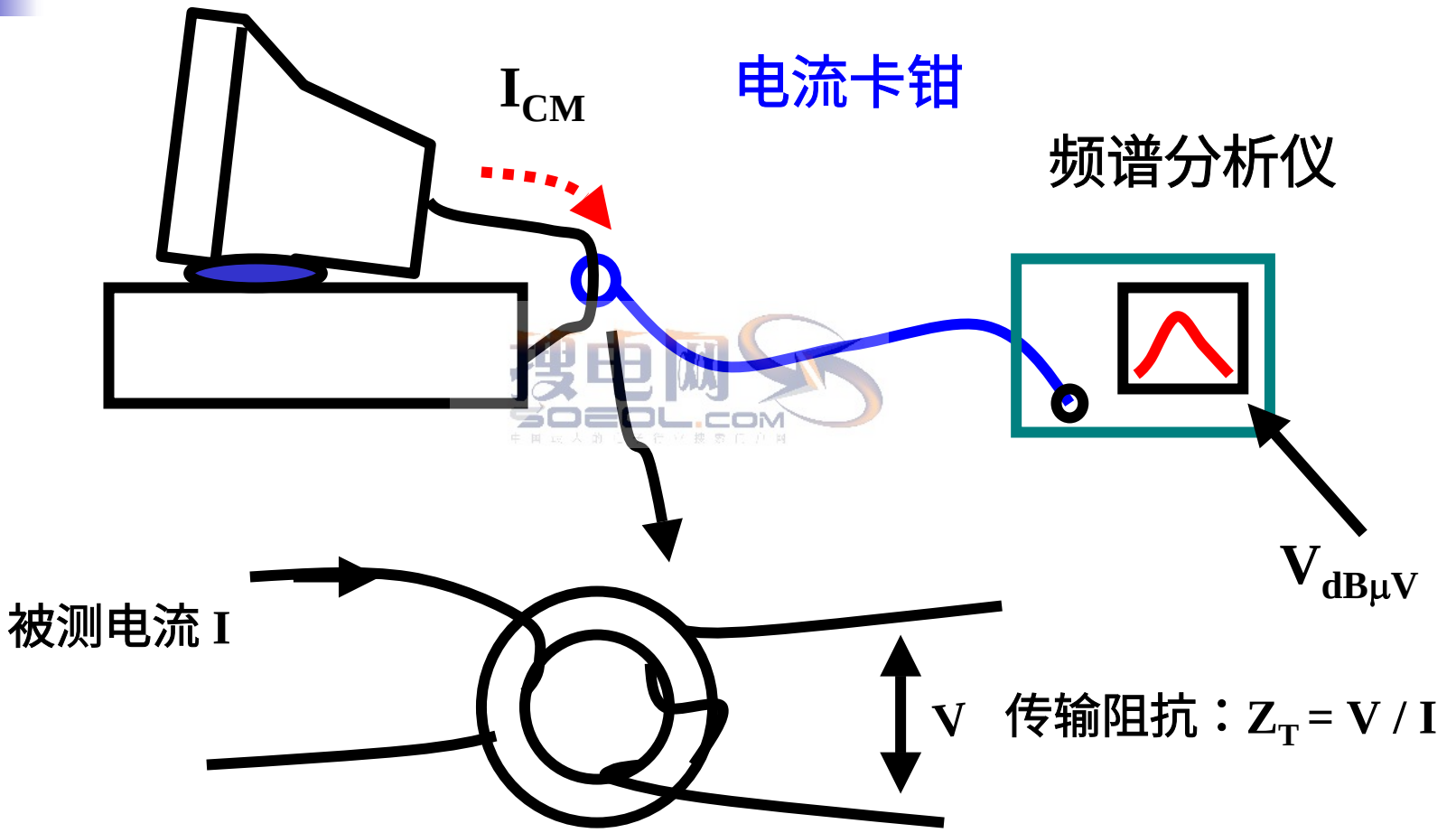
近场区内: $E = 1430 I L / (f D^3)$ μV/m

远场区内: $E = 0.63 I L f / D$ μV/m

考虑地面反射： $E = 1.26 I L f / D$ μV/m

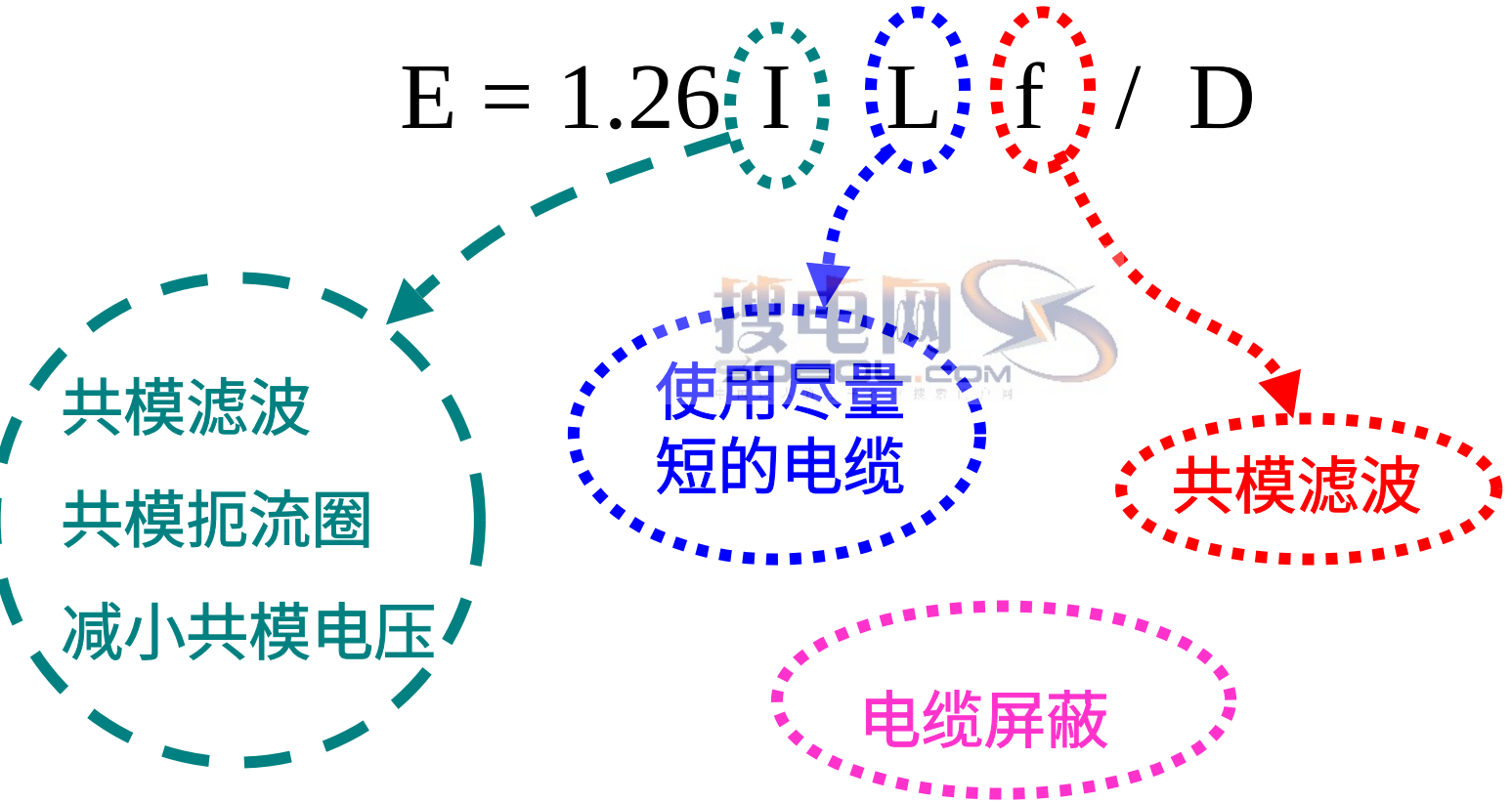
L >λ/2或λ/4时： $E = 120 I / D$ μV/m

共模电流的测量

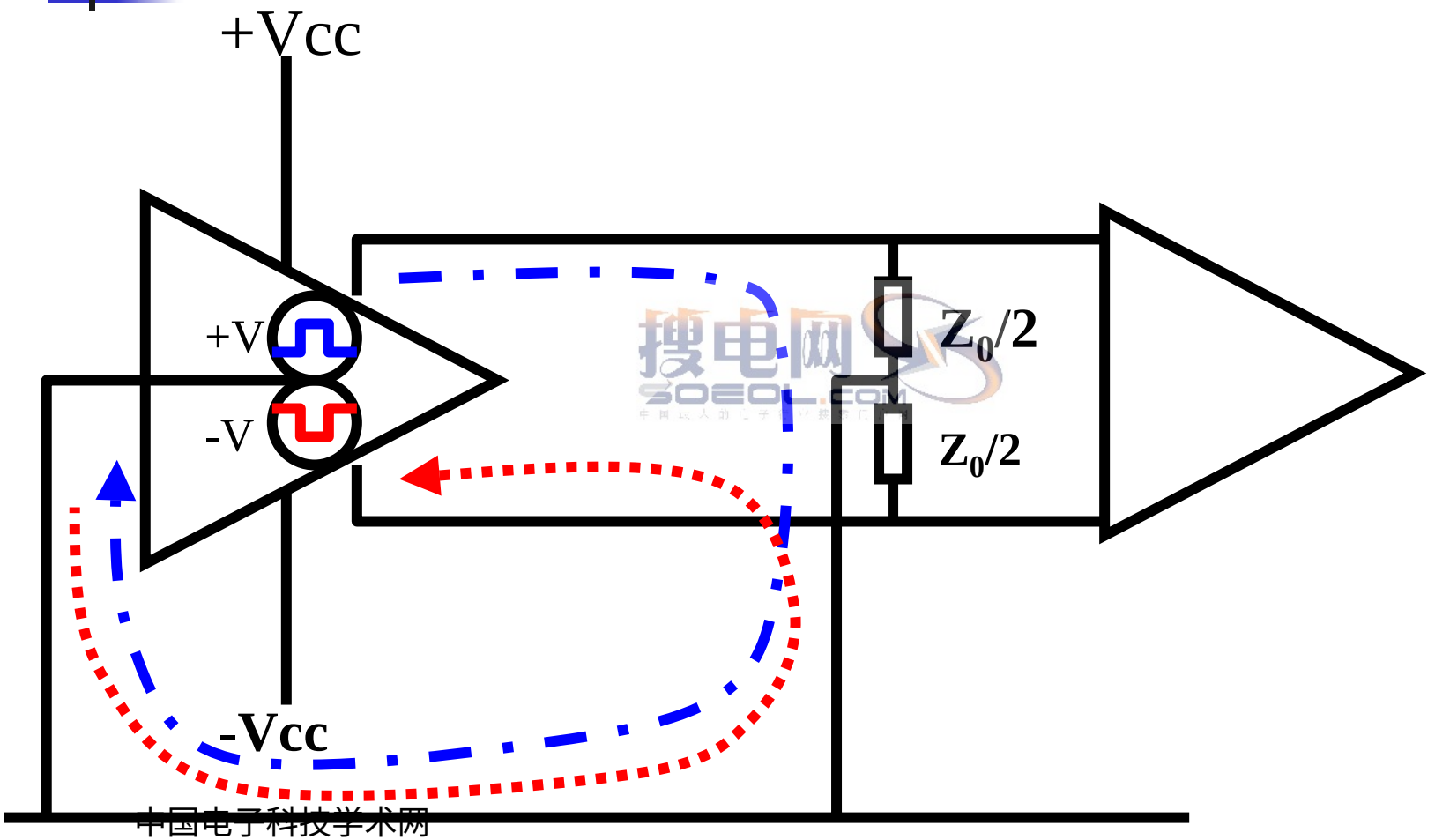


怎样减小共模辐射

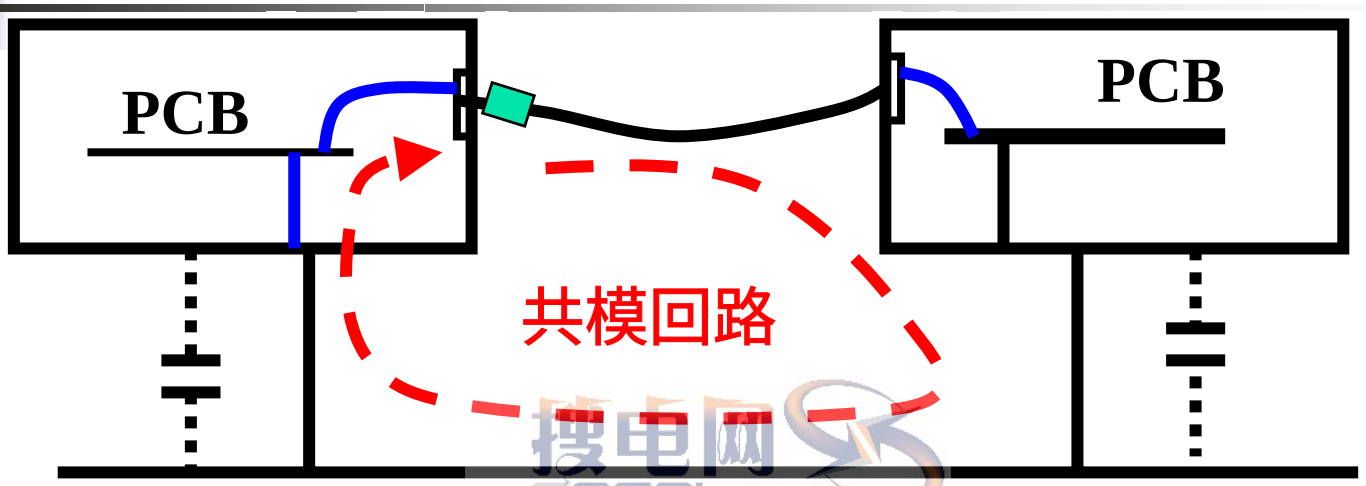
$$E = 1.26\ I\ L\ f\ /\ D$$



平衡接口电路



增加共模回路的阻抗



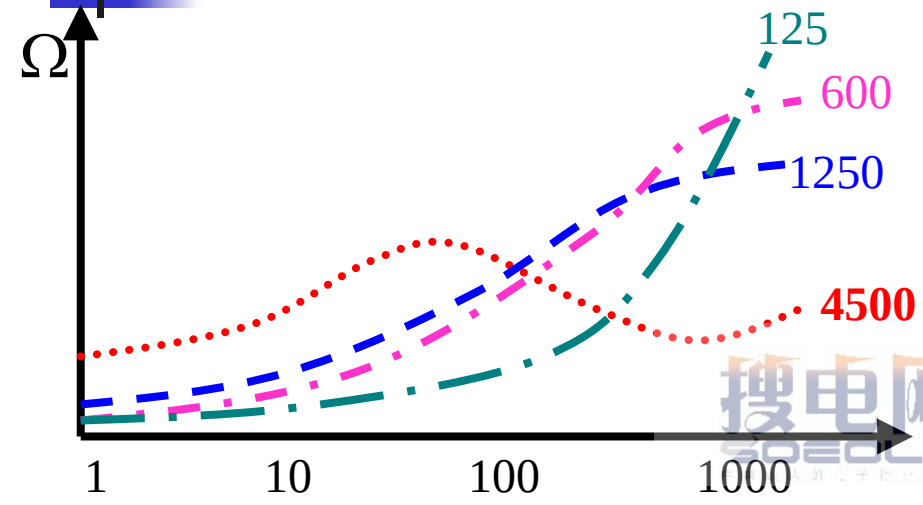
改善量 = $20\lg(E_1 / E_2) = 20\lg(I_{CM1} / I_{CM2})$

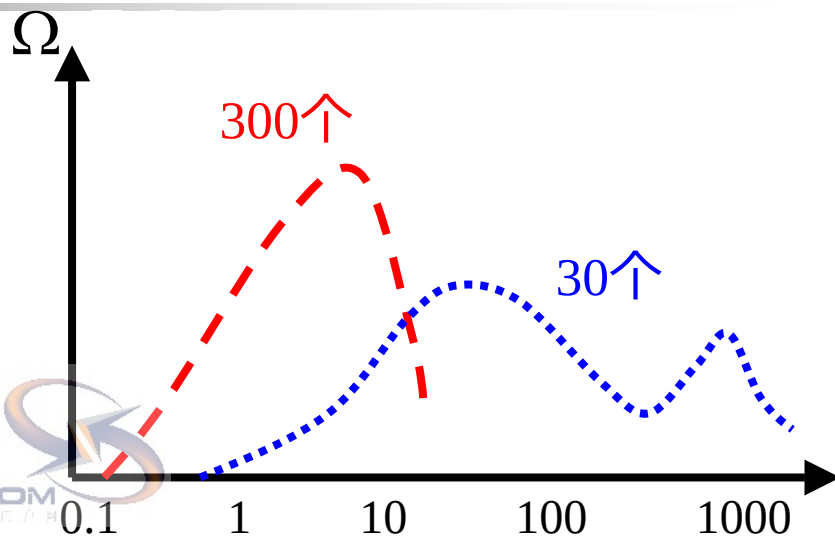
$= 20\lg[(V_{CM} / Z_{CM1}) / (V_{CM} / Z_{CM2})]$

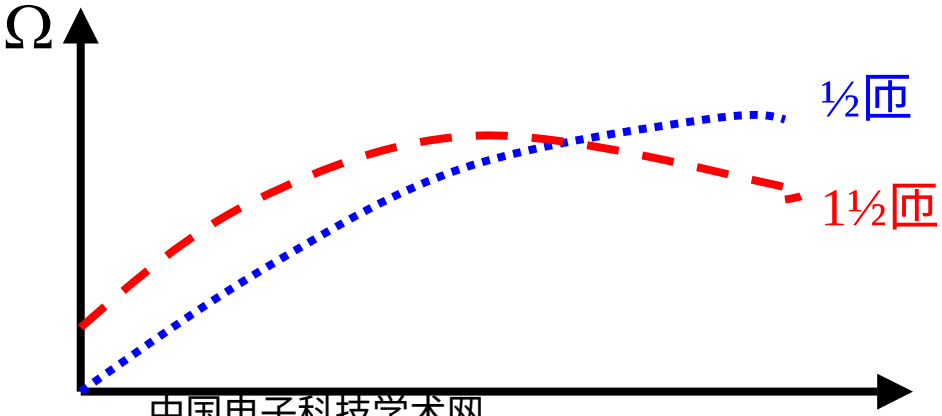
$= 20\lg(Z_{CM2} / Z_{CM1})$

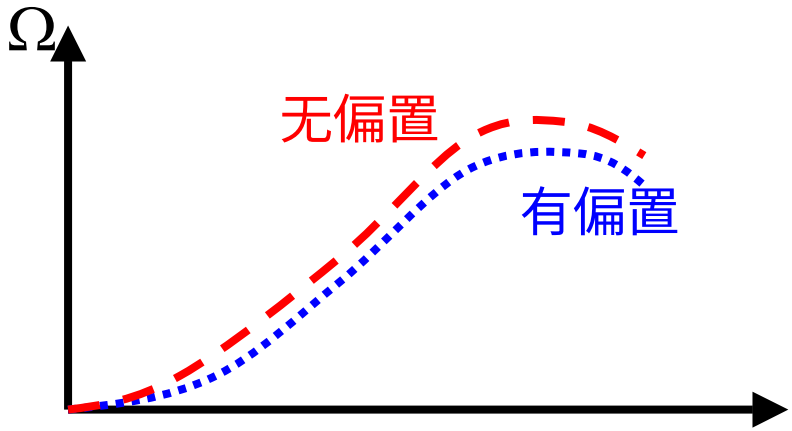
$= 20\lg(1 + Z_L / Z_{CM1})$ dB

铁氧体磁环使用方面的一些问题

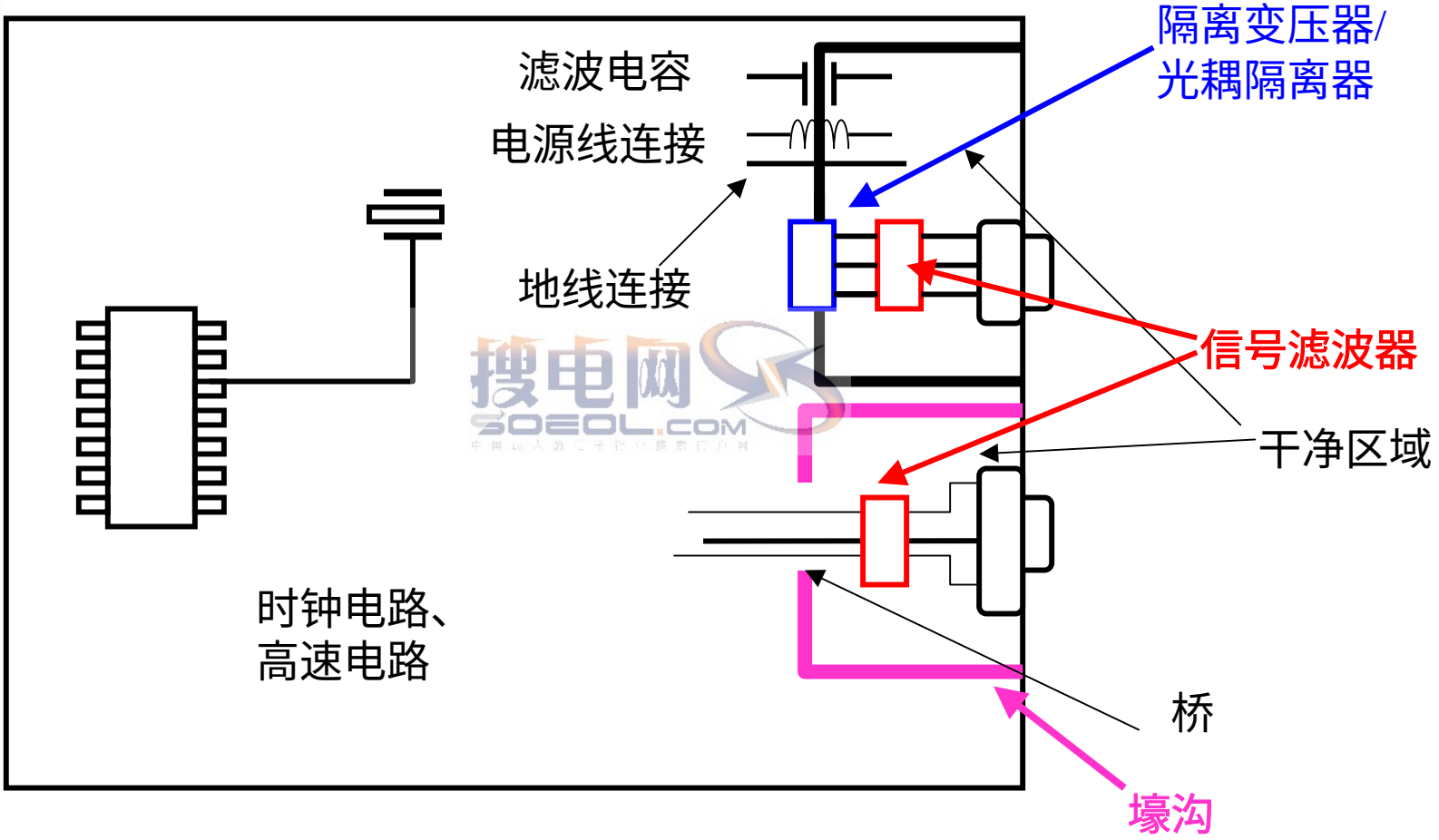




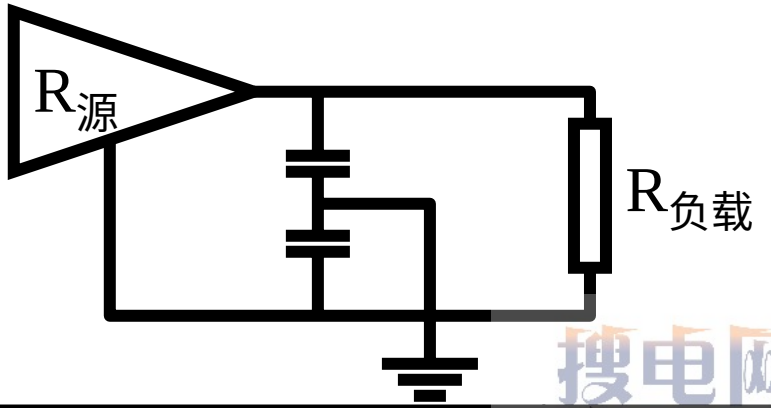


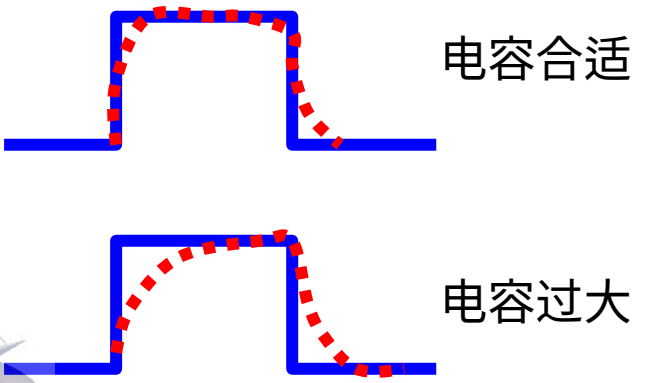


I/O接口布线的一些要点



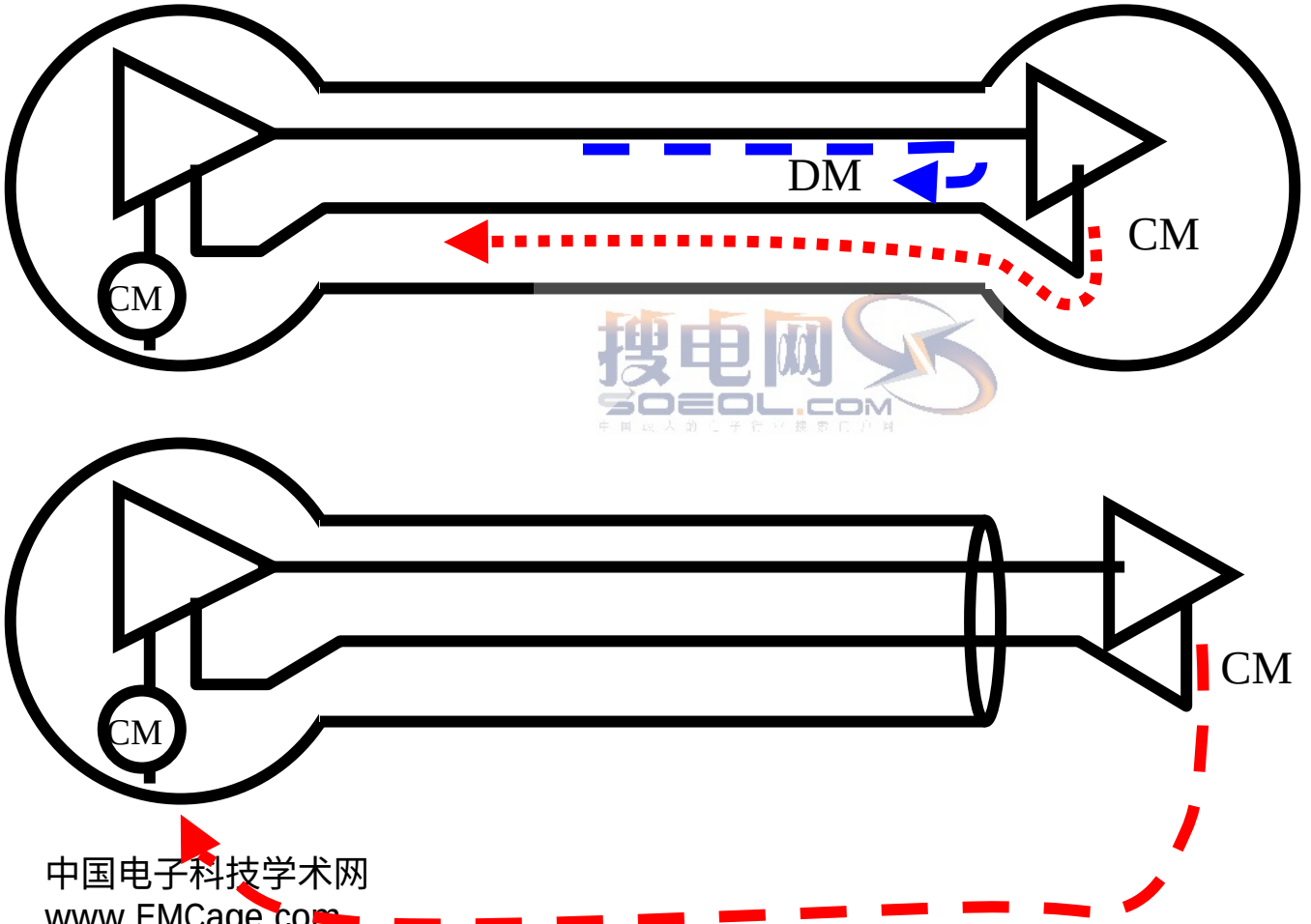
滤波器电容量的选择



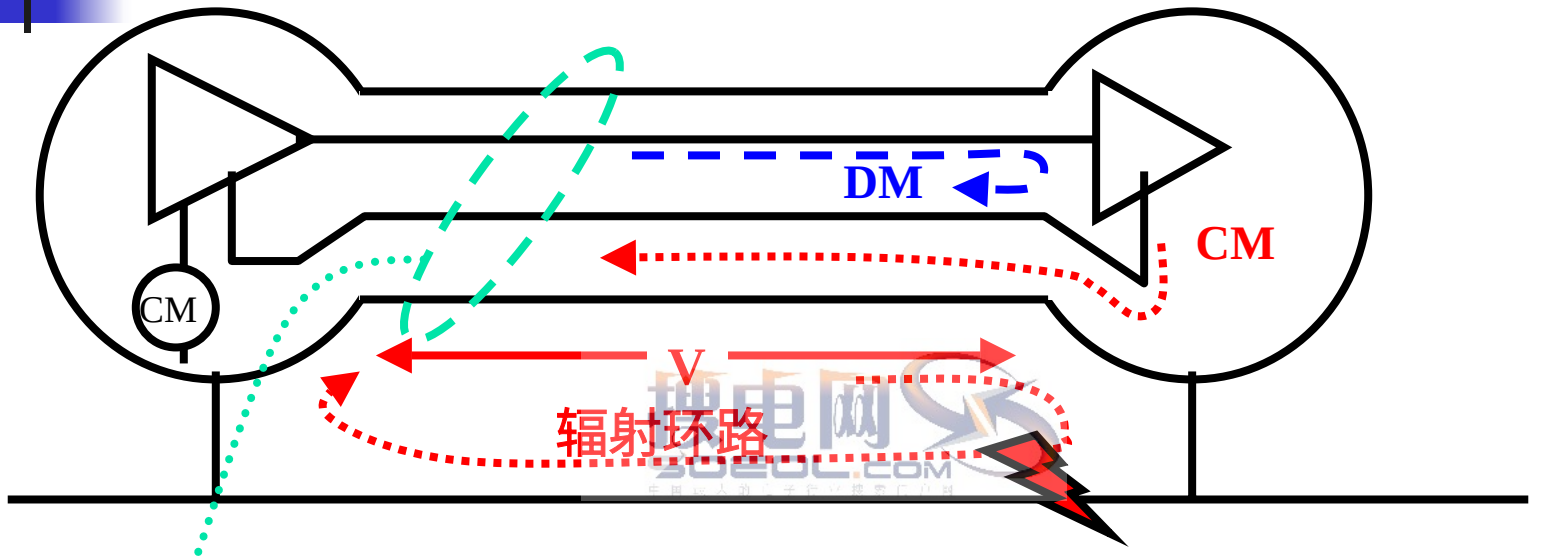


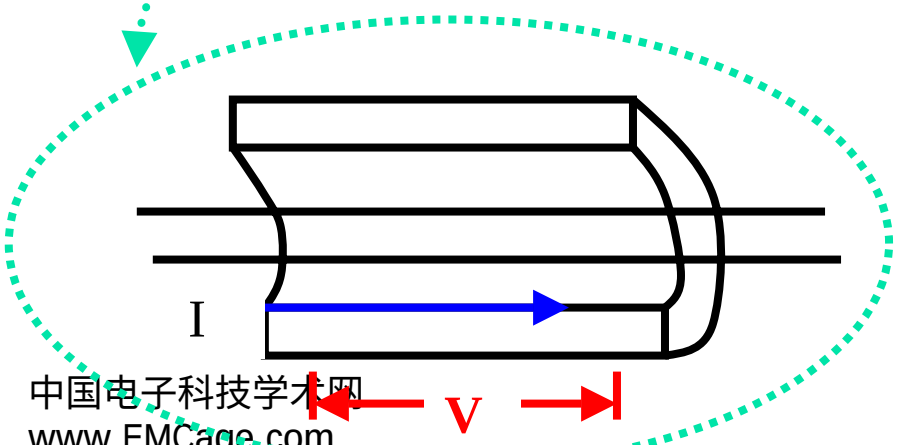
	低速接口 10 ~ 100kB/s	高速接口 2MB/s	低速CMOS	TTL
上升时间 tr	0.5~1μs	50ns	100ns	10ns
带宽 BW	320kHz	6MHz	3.2MHz	32MHz
总阻抗 R	120Ω	100Ω	300Ω	100~150Ω
最大电容C	2400pF	150pF	100pF	30pF

用屏蔽电缆抑制共模辐射



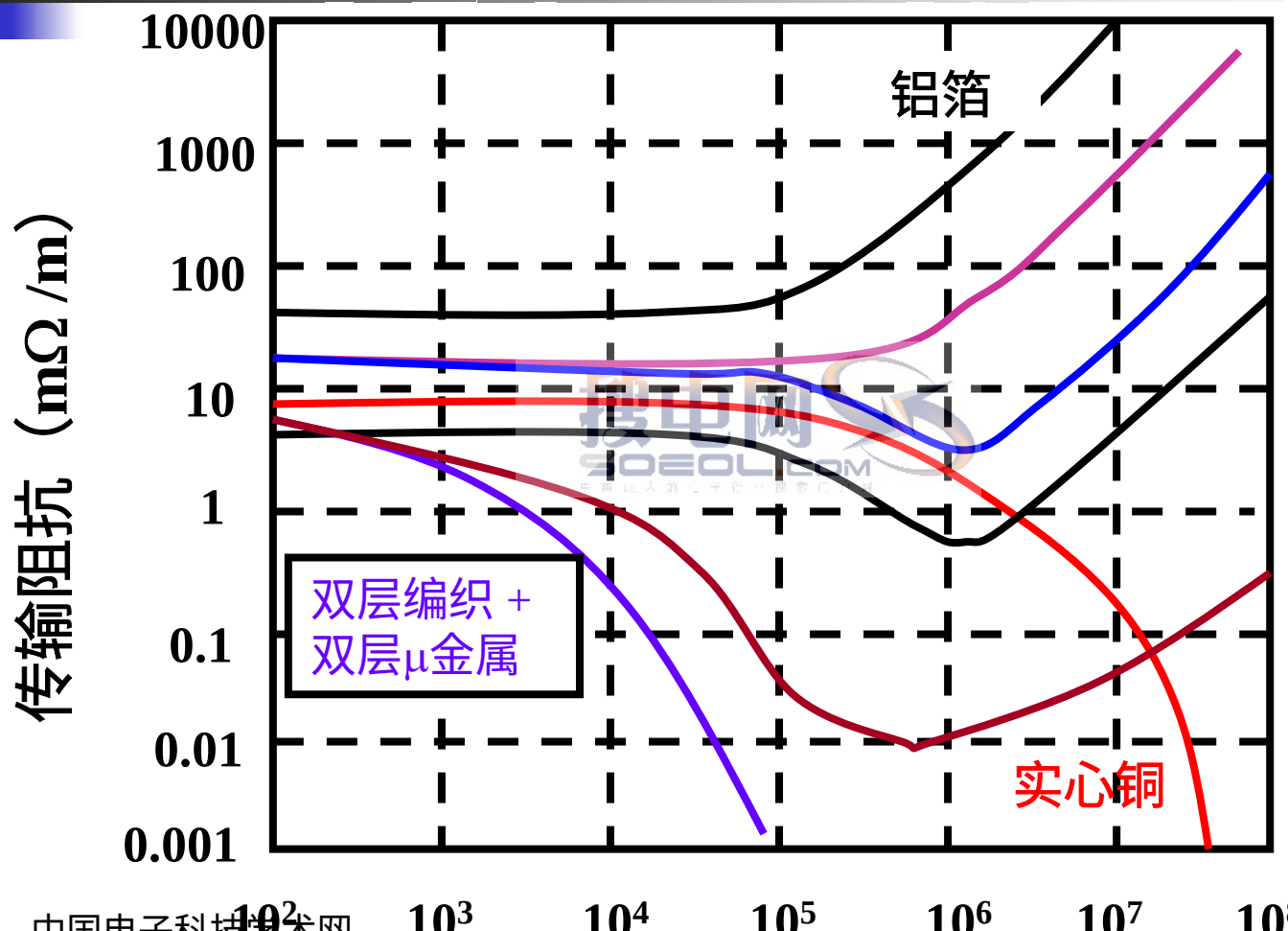
屏蔽电缆的评估





$$Z_T = V / I$$

不同屏蔽层的传输阻抗



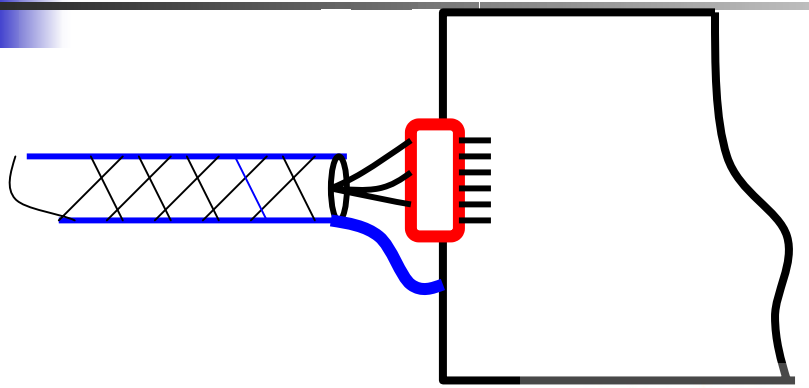
单层编织

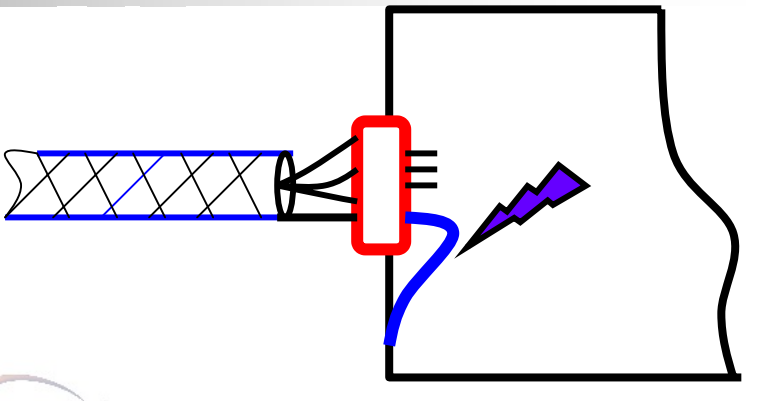
最佳单层编织

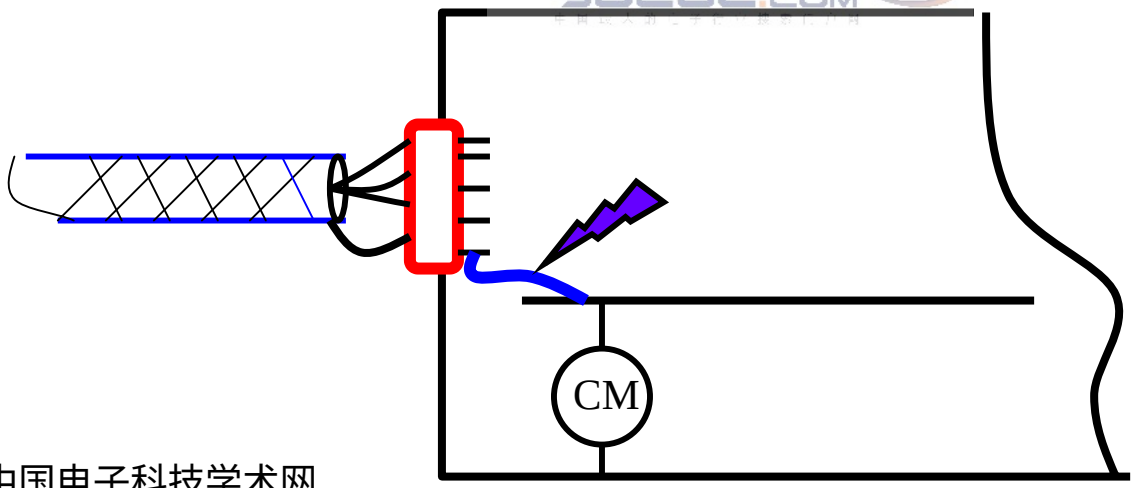
双层编织

双层编织 +
一层μ金属

屏蔽层的错误接法

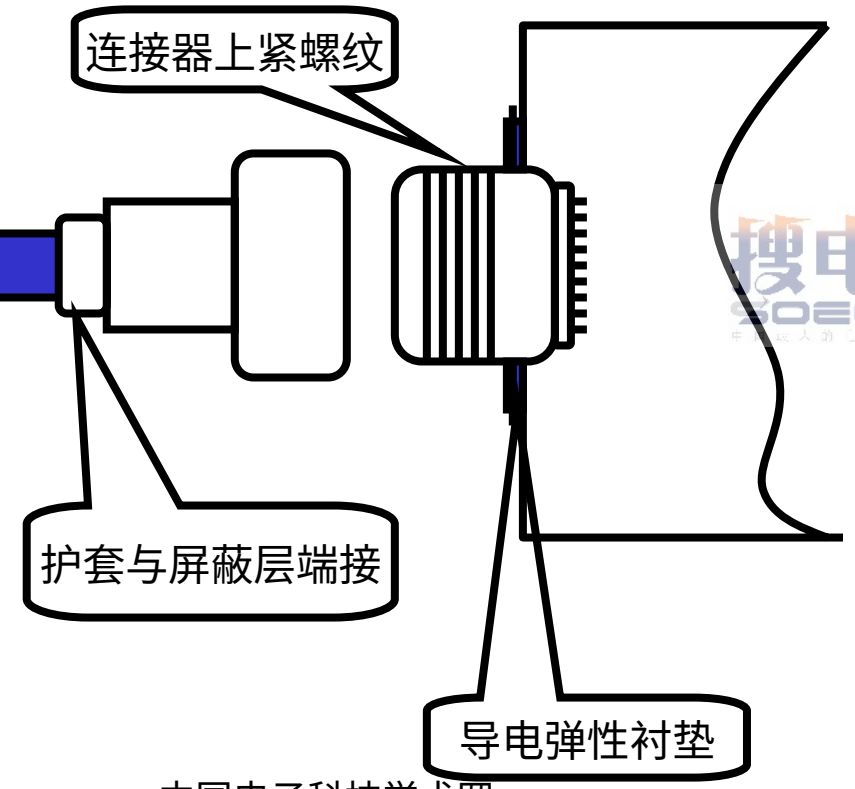




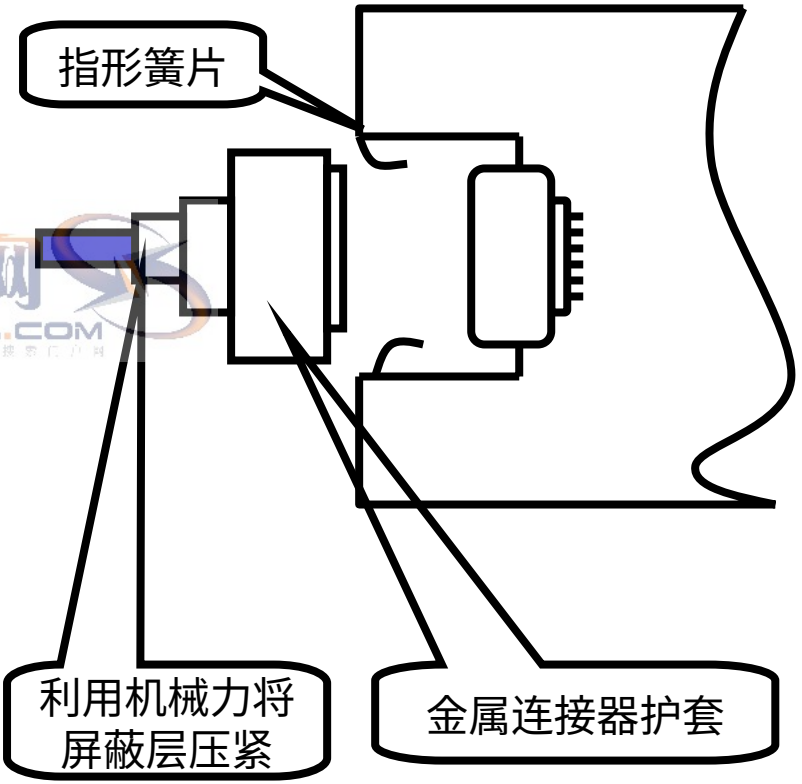


电缆屏蔽层的正确端接

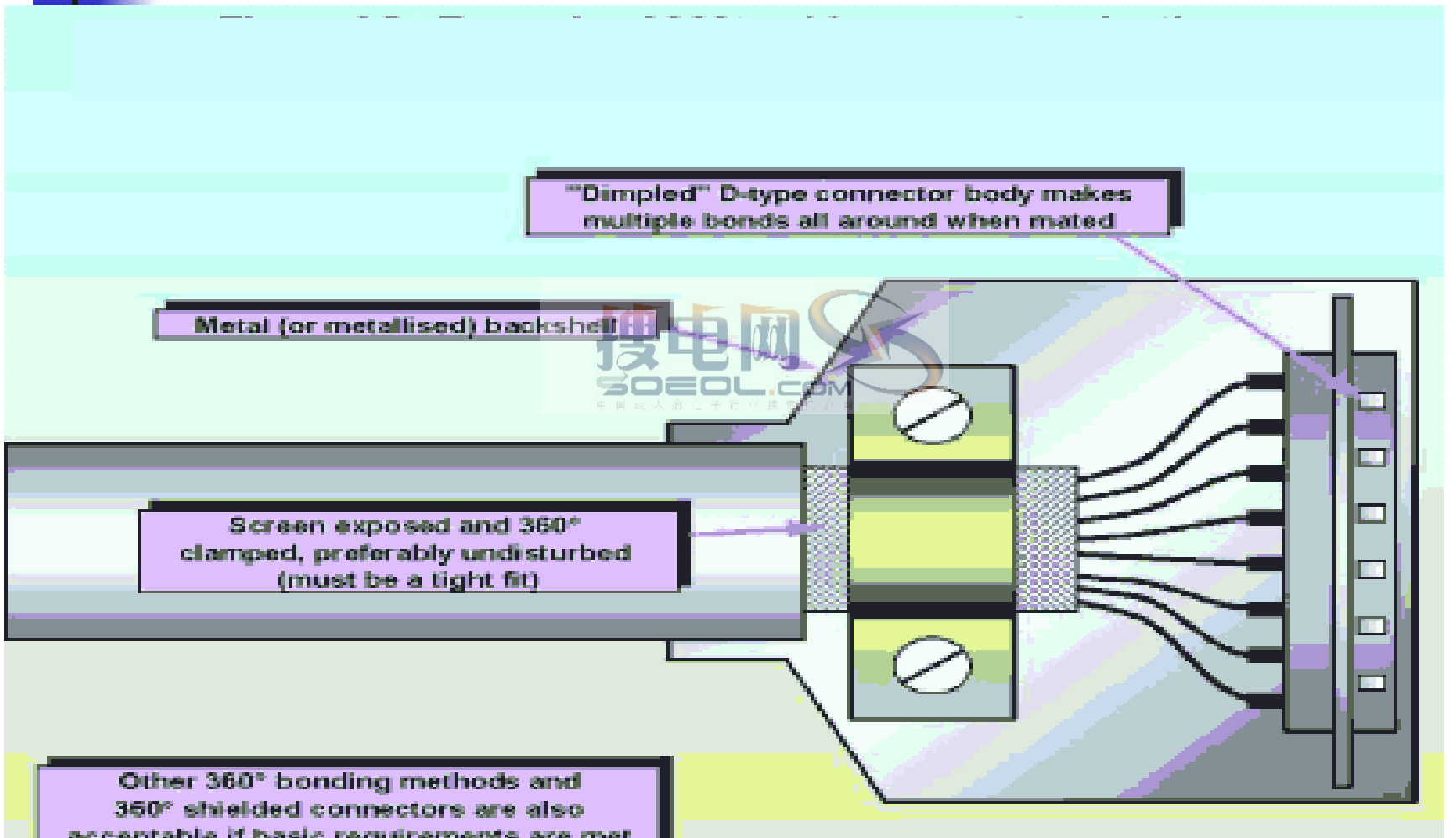
航空连接器



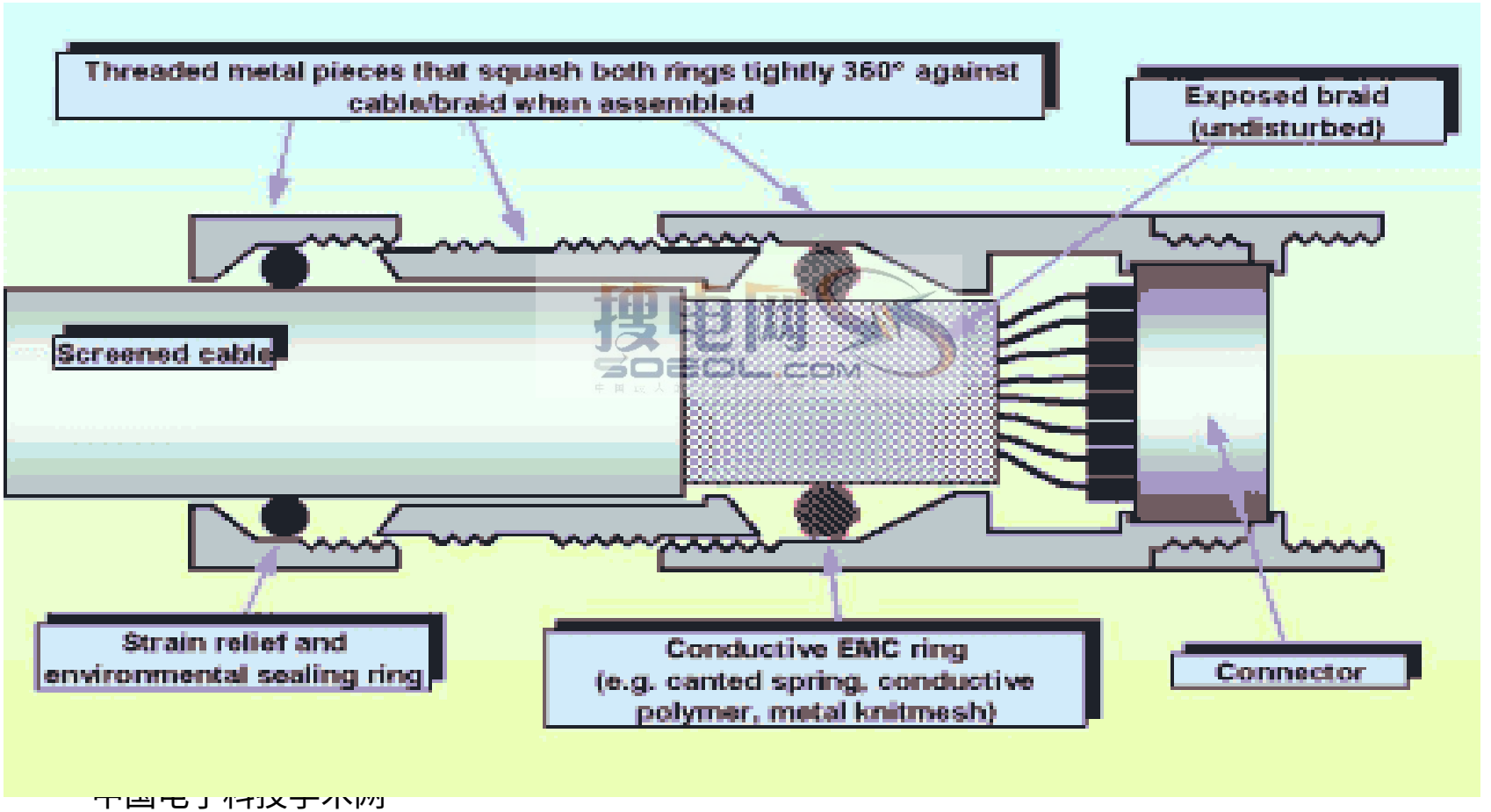
D形连接器



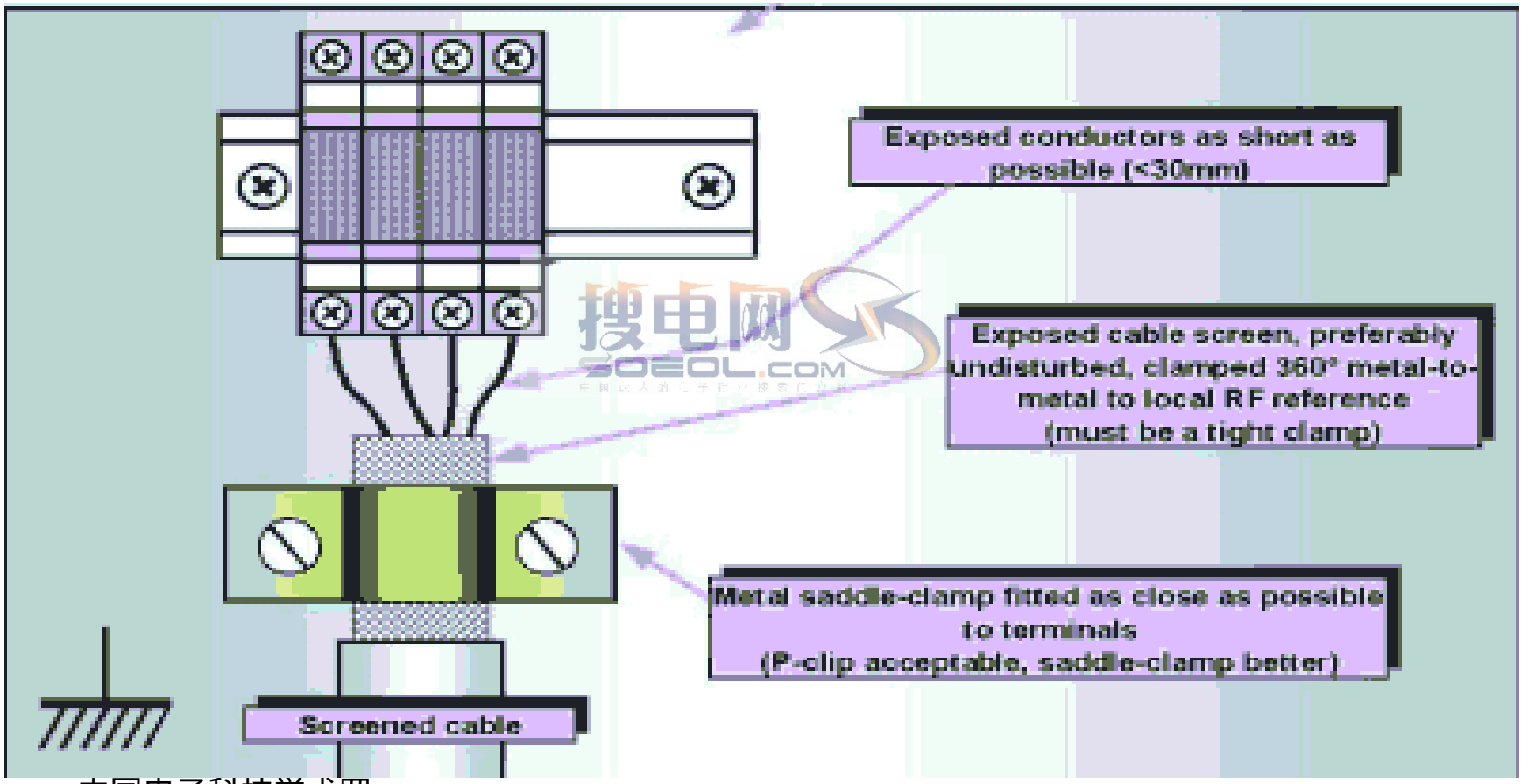
D型连接器的屏蔽层搭接



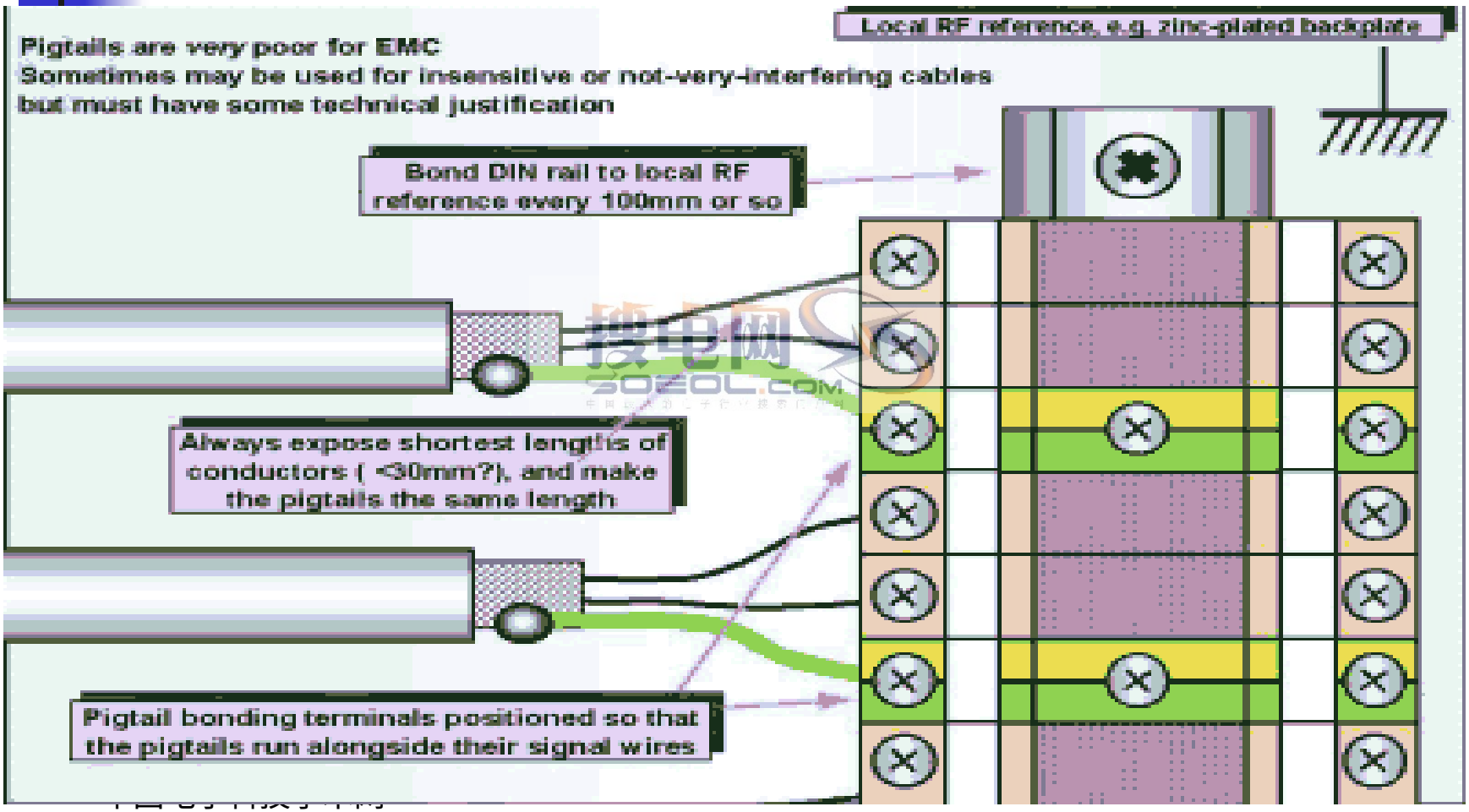
圆形连接器屏蔽层搭接



接线端子上的屏蔽电缆



尽量减小小辫接法的危害



线路板上的局部屏蔽