

Errata for the  
PCI Express Base Specification, Revision 1.1

Updated Feb 2007

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***Errata for the PCI Express Base Specification, Revision 1.1***

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## Table Of Contents

C1.	Class Code Reassignment.....	5
C2.	Interaction of "No Snoop" Attribute in TLPs and "Reject Snoop Transactions" .....	5
C3.	Appendix D Clarifications .....	5
C4.	Form Factors Not Requiring Beacon .....	6
C5.	EP and TLPs Without Data <b>(UPDATED)</b> .....	6
C6.	PCI-PM L1 & Completion Timeout.....	7
C7.	Unsupported Request Equivalency to Master Abort .....	7
C8.	Switch and Root Port Virtual Bridge Behavior in Non-D0 States ....	8
C9.	Expectations About Unexpected Completions .....	8
C10.	Switch Handling of 101b Routing Code .....	9
C11.	Root Complex Minimum Credit Requirement.....	9
C12.	TLP Acceptance Rules .....	10
C13.	Ports Must Remain Disabled While Disabled Bit is Set.....	10
C14.	CLKREQ# Allows Platform Refclock Removal in L1 .....	11
C15.	Assorted Register Clarifications <b>(UPDATED)</b> .....	11
C16.	Assorted .....	19
C17.	FC Advertisement Check Not Actually Possible.....	21
C18.	AckNak_LATENCY_TIMER Clarifications .....	22
C19.	Assorted .....	25
C20.	REPLAY_TIMER Clarifications .....	26
C21.	Text Updates for Trusted Configuration .....	30
C22.	L1 Invocation Example .....	30
C23.	L1, L23_Ready Negotiation .....	30

<b>C24.</b>	<b>Retrain Link Bit Only Exists for Upstream Components.....</b>	<b>32</b>
<b>C25.</b>	<b>Definition of Completer .....</b>	<b>32</b>
<b>C26.</b>	<b>ECRC Rules.....</b>	<b>33</b>
<b>C27.</b>	<b>Redundant Example in Section 2.2.6.2. ....</b>	<b>34</b>
<b>C28.</b>	<b>Scope of TC Service Policy.....</b>	<b>34</b>
<b>C29.</b>	<b>PM Messages and BDF/BD .....</b>	<b>34</b>
<b>C30.</b>	<b>VC Capability Is Indeed Optional.....</b>	<b>35</b>
<b>C31.</b>	<b>INTx Interrupt Status Clarification.....</b>	<b>36</b>
<b>C32.</b>	<b>Reserved Fields in “2” Registers .....</b>	<b>36</b>
<b>C33.</b>	<b>Device Status Register Error Detected Bit Typos.....</b>	<b>37</b>
<b>C34.</b>	<b>D0active.....</b>	<b>37</b>
<b>C35.</b>	<b>Assorted .....</b>	<b>38</b>
<b>C36.</b>	<b>Unexpected Completion Sometimes Function-Specific.....</b>	<b>41</b>

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## C1. Class Code Reassignment

SWWG Approved 1 August 2005 -- Release Date: 1 August 2005

In Section 1.3.4 of the PCI Express Base Specification 1.1 and the Integrated Devices – Event Collector ECN to the 1.0a:

5       □ A Root Complex Event Collector has the Base Class 08h, Sub-Class ~~05h~~06h and Programming Interface 00h.

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## C2. Interaction of "No Snoop" Attribute in TLPs and "Reject Snoop Transactions"

PWG Approved 16 June 2005 -- Release Date: 1 August 2005

In Table 7-40: VC Resource Capability Register, change:

15       **Reject Snoop Transactions** – When set to zero, transactions with or without the No Snoop bit set within the TLP Header are allowed on this VC. When set to 1, any transaction ~~for which the No Snoop attribute is applicable but is not set without the No Snoop bit set~~ within the TLP Header will be rejected as an Unsupported Request. See Section 2.2.6.5 for information on where the No Snoop attribute is applicable. This field is valid for Root Ports and RCRB; it is not valid for PCI Express Endpoint devices or Switch Ports.

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## C3. Appendix D Clarifications

PWG Approved 16 June 2005 -- Release Date: 1 August 2005

In Appendix D, change text:

25       ~~“This document The PCI Express Base Specification does not specify the allowed rules governing the creation of resource dependencies between TLPs using different Traffic Classes. Such dependencies~~ Dependencies between packets in different Traffic Classes can create potential deadlock if devices make different assumptions about what is allowed and what is not. Dependencies can be created when a packet is forwarded (transmitted verbatim) or translated (transmitted with modification) from an input port to an output port.

30       Resource dependencies are created when received packets are ~~either~~ forwarded/translated and retransmitted on the same or a different link. Due to the fact that the forwarding/translating device has finite buffer resources, this behavior creates a dependency ~~upon~~ between the ability to receive a packet ~~on and~~ the ability to transmit a packet (in potentially a different VC or sub-channel).”

...

“This means:

a request in sub-channel X(TC=m) is ~~translated~~/forwarded/translated in sub-channel Y(TC=n). n and m are between 0-7. X and Y are either P (Posted Request), N (Non-Posted Request), or C (Completion).”

35       ...

“A Switch ~~will not~~ **is not allowed to** modify the TLPs that flow through it, but must ensure complete independence of resources assigned to separate VCs. System software must comprehend the system dependency rules when configuring TC/VC mapping throughout the system.”

...

40 "One possible legal mapping ~~ismight be:~~"

...

45 “Others ~~of these~~ potential dependencies may be legal when comprehended as part of a specific usage model. For example, these cases: P(m) ->P(n), N(m) -> N(n), P(m) -> N(n), N(m) -> P(n) where m! = n might exist where a device **processes services** incoming requests ~~to complete those requests~~ by issuing modified versions of those requests using a different Traffic Class (for example, remapping the first request's address and generating the new request with the resulting address). In these cases, suitable rules must be applied to prevent circular dependencies that would lead to deadlock or livelock.”

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## **C4. Form Factors Not Requiring Beacon**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

50 *In Section 5.3.3.2, change;*

The Link wakeup mechanisms provide a means of signaling the platform to re-establish power and reference clocks to the components within its domain. There are two defined wakeup mechanisms: Beacon and WAKE#. The Beacon mechanism uses in-band signaling to implement wakeup functionality, and is described in Section 4.3.2.4. For components that support wakeup functionality, ~~Beacon is the required mechanism for all components, except for components designed exclusively for the following~~ **the form factor specification(s) targeted by the implementation determine the wakeup mechanism support requirements. - PCI Express Card Electromechanical Specification and Mini PCI Express Card Electromechanical Specification.**

...

60 The WAKE# mechanism uses sideband signaling to implement wakeup functionality. WAKE# is an “open drain” signal asserted by components requesting wakeup and observed by the associated power controller. WAKE# is only defined for certain form factors, and the detailed specifications for WAKE# are included in the relevant form factor specifications. Specific form factor specifications may require the use of either Beacon or WAKE# as the wakeup mechanism. ~~All form factors that require WAKE# as the wakeup mechanism must permit components to also generate Beacon, although the Beacon may not be observed.~~

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## **C5. EP and TLPs Without Data (UPDATED)**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005; Updated 8 February 2007**

*In Section 2.7.2.2, change:*

Data poisoning applies only to the data within a Write Request (Posted or Non-Posted) or a Read Completion.

70 Poisoning of a TLP is indicated by a 1b value in the EP field

~~Transmitters are permitted to set the EP field to 1b only for TLPs that include a data~~ **payload.**

~~The behavior of the receiver is not specified if the EP bit is set for any TLP that does not include a data~~ **payload.**

If a Transmitter supports data poisoning, TLPs that are known to the Transmitter to include bad data must use the poisoning mechanism defined above.

75 Receipt of a Poisoned TLP is a reported error associated with the Receiving device/function (see Section 6.2)

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## **C6. PCI-PM L1 & Completion Timeout**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

*In Section 5.3.2.1, Entry into the L1 State:*

80 When two components' interconnecting Link is in L1 as a result of the Downstream component being programmed to a non-D0 state, both components suspend the operation of their Flow Control Update, ~~TLP Completion Timeout~~, and, if implemented, Update FCP Timer (see Section 2.6.1.2) counter mechanisms. Refer to Chapter 4 for more detail on the Physical Layer behavior.

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## **C7. Unsupported Request Equivalency to Master Abort**

85 **PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

*In Section 2.3.1, add implementation note as shown:*

...

If the Request Type is not supported (by design or because of configuration settings) by the device, the Request is an Unsupported Request, and is reported according to Section 6.2

90 If the Request requires Completion, a Completion Status of UR is returned (see Section 2.2.9)



### **IMPLEMENTATION NOTE**

#### **When Requests are Terminated Using Unsupported Request**

95 In Conventional PCI, a device “claims” a request on the bus by asserting DEVSEL#. If no device claims a request after a set number of clocks, the request is terminated as a Master Abort. Because PCI Express is a point to point interconnect, there is no equivalent mechanism for claiming a request on a link, since all transmissions by one component are always sent to the other component on the link. Therefore, it is necessary for the receiver of a request to determine if the request should be “claimed”. If the request is not claimed, then it is handled as an Unsupported Request, which is the PCI Express equivalent of conventional PCI’s Master Abort termination. In general, one can determine the correct behavior by asking the question: *Would the device assert DEVSEL# for this request in conventional PCI?*

105 For devices with Type 0 headers (all types of Endpoints), it is relatively simple to answer this question. For Memory and IO Requests, this determination is based on the address ranges the device has been programmed to respond to. For Configuration requests, the Type 0 request format indicates the device is by definition the “target”, although the device will still not claim the Configuration Request if it addresses an unimplemented function.

110 For devices with Type 1 headers (Root Ports, Switches and Bridges), the same question can generally be applied, but since the behavior of a conventional PCI bridge is more complicated than that of a Type 0 device, it is somewhat more difficult to determine the answers. One must consider Root Ports and Switch ports as if they were actually composed of conventional PCI to PCI bridges, and then at each stage consider the configuration settings of the virtual bridge to determine the correct behavior.

PCI Express Messages do not exist in conventional PCI, so the above guideline cannot be applied. This specification describes specifically for each type of Message when a device must handle the request as an Unsupported Request. Messages pass through Root and Switch ports unaffected by conventional PCI control mechanisms including Bus Master Enable & power state setting.

115 Note that Completer Abort, which is the PCI Express equivalent to Target Abort, is used only to indicate a serious error that makes the completer permanently unable to respond to a request that it would otherwise have normally responded to. Because Target Abort is used in conventional PCI only when a target has asserted DEVSEL#, is incorrect to use Completer Abort for any case where a conventional PCI target would have ignored a request by not asserting DEVSEL#.

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## **C8. Switch and Root Port Virtual Bridge Behavior in Non-D0 States**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

*At the end of Section 5.3.1., add implementation note as shown:*

... this specification takes precedence for PCI Express components and Link hierarchies.

125



### **IMPLEMENTATION NOTE**

#### **Switch and Root Port Virtual Bridge Behavior in Non-D0 States**

130 When a Type 1 device associated with a Switch/Root Port, a “virtual bridge”, is in a non-D0 power state, it will emulate the behavior of a conventional PCI bridge in its handling of Memory, IO and Configuration Requests and Completions. All Memory and IO requests flowing downstream are terminated as Unsupported Requests. All Type 1 Configuration Requests are terminated as Unsupported Requests, however Type 0 Configuration Request handling is unaffected by the virtual bridge D state. Completions flowing either direction across the virtual bridge are unaffected by the virtual bridge D state.

Note that the handling of PCI Express Messages is not affected by the PM state of the virtual bridge.

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## **C9. Expectations About Unexpected Completions**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**



In Section 2.3.2, Completion Handling Rules:

140 When a device receives a Completion which does not ~~match the Transaction ID for~~~~respond to~~ any of the outstanding Requests issued by that device, the Completion is called an “Unexpected Completion.”

- ❑ If a received Completion is not malformed and matches the Transaction ID of an outstanding Request, but in some other way does not match the corresponding Request, it is permitted for the receiver to handle the Completion as an Unexpected Completion

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145 **C10. Switch Handling of 101b Routing Code**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

In Section 2.3, add:

150 . . .  
If the value in r[2:0] indicates the Msg/MsgD terminates at the Receiver (100b or a reserved value), or if the Message Code field value is defined and corresponds to a Message which must be comprehended by the Switch, the Switch must process the Message according to the Message processing rules

If the value in r[2:0] indicates Gathered and routed to Root Complex (101b), see Section 5.3.3.2.1 for Message handling rules

155 It is an error to receive any Msg/MsgD Request other than a PME\_TO\_Ack that specifies 101b routing. It is an error to receive a PME\_TO\_Ack at the Upstream Port of a Switch. Switches may check for violations of these rules – TLPs in violation are Malformed TLPs. If checked, this is a reported error associated with the Receiving Port (see Section 6.2)

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160 **C11. Root Complex Minimum Credit Requirement**

**PWG Approved 16 June 2005 -- Release Date: 1 August 2005**

In Section 2.6.1:

Table 2-27: Minimum Initial Flow Control Advertisements<sup>14</sup>

Credit Type	Minimum Advertisement
...	
CPLD	Root Complex (supporting peer-to-peer traffic between all Root Ports) and Switch: Largest possible setting of the Max_Payload_Size for the component divided by FC Unit Size, <del>or the size of the largest Read Request the component will ever generate, whichever is smaller.</del> Root Complex (not supporting peer-to-peer traffic between all Root Ports) and Endpoint: infinite FC units - initial credit value of all 0s

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## C12. TLP Acceptance Rules

PWG Approved 30 March 2006 -- Release Date: 8 May 2006

In Section 2.4.1, change:

- ❑ For Root Ports and Switch Downstream Ports, acceptance of a Posted Request or Completion must not depend upon the transmission of a Non-Posted Request within the same traffic class [ref footnote below].
- 170 ❑ For Switch Upstream Ports, acceptance of a Posted Request or Completion must not depend upon the transmission on a downstream port of Non-Posted Request within the same traffic class [ref footnote below].
- ❑ For Endpoint, Bridge and Switch Upstream Ports, the acceptance of a Posted Request must not depend upon the transmission of any TLP from that same upstream port within the same traffic class [ref footnote below].
- 175 ❑ For Endpoint, Bridge and Switch Upstream Ports, the acceptance of a Non-Posted Request must not depend upon the transmission of a Non-Posted Request from that same upstream port within the same traffic class [ref footnote below].
- ❑ For Endpoint, Bridge and Switch Upstream Ports, the acceptance of a Completion must not depend upon the transmission of any TLP from that same upstream port within the same traffic class [ref footnote below].
- 180 ❑ Note that Endpoints are never permitted to block acceptance of a Completion
- ~~❑ For Endpoints and Bridges acceptance of a posted or non-posted request must not depend upon the transmission of a posted or non-posted request in the same Traffic Class.~~
- ~~❑ Acceptance of a posted request must not depend upon the transmission of a completion in the same Traffic Class.~~
- 185 ❑ Completions issued for ~~a~~Non-~~p~~Posted ~~r~~Requests must be returned in the same Traffic Class as the corresponding ~~a~~Non-~~p~~Posted ~~r~~request.
- ~~❑ Acceptance of a completion must not depend upon the transmission of a posted or non-posted request or a completion in the same Traffic Class.~~
- 190 ❑ Root Complexes that support peer-to-peer operation ~~on~~ and Switches must enforce these transaction ordering rules for all forwarded traffic.

Add footnote:

- 195 1 Satisfying the above rules is a necessary, but not sufficient condition to ensure deadlock free operation. Deadlock free operation is dependent upon the system topology, the number of virtual channels supported and the configured traffic class to virtual channel mappings. Specification of platform and system constraints to ensure deadlock free operation is outside the scope of this specification (see Appendix D for a discussion of relevant issues).

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## C13. Ports Must Remain Disabled While Disabled Bit is Set

EWG Approved 30 March 2006 -- Release Date: 8 May 2006

*In Section 4.2.6.9. Disabled, change:*

...

❑ If an Electrical Idle ordered set was transmitted and received (even while transmitting TS1 with the Disable Link bit asserted), then:

205

- LinkUp = 0 (False)

- ◆ Note: At this point, the Lanes are considered Disabled.

- ~~• The next state is Detect when directed or if Electrical Idle is exited.~~

- For Downstream components: The next state is Detect when Electrical Idle exit is detected at the Receiver.

210

- For Upstream components: The next state is Detect when directed (e.g. when the Link Disable bit is set to 0b by software).

❑ ~~Otherwise,~~ For Downstream components, if no Electrical Idle ordered set is received after a 2 ms timeout, the next state is Detect.

215

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### ***C14. CLKREQ# Allows Platform Refclock Removal in L1***

**PWG Approved 30 March 2006 -- Release Date: 8 May 2006**

*In Section 5.2, change:*

...

❑ L1 – Higher latency, lower power “standby” state.

220

❑ L1 support is required for PCI-PM compatible power management. L1 is optional for ASPM unless specifically required by a particular form factor.

All platform provided main power supplies ~~and component reference clocks~~ must remain active at all times during L1. All platform provided component reference clocks must remain active at all times during L1, except as permitted by Clock Power Management (using CLKREQ#) when enabled. The component’s internal PLLs may be shut off during L1, enabling greater energy savings at a cost of increased exit latency.

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...

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### ***C15. Assorted Register Clarifications (UPDATED)***

**SWWG/PWG Approved 5 May 2006/30 March 2006 -- Release Date: 8 May 2006**

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**Update PWG Approved 15 June 2006 -- Release Date: 25 August 2006**

In Section 7.5.1.1, edit as shown:

7.5.1.1. Command Register (Offset 04h)

235 Table 7-3 establishes the mapping between PCI 3.0 and PCI Express for PCI 3.0 configuration space Command register.

Table 7-3: Command Register

Bit Location	Register Description	Attributes
...		
10	<p><b>Interrupt Disable</b> – Controls the ability of a PCI Express Function device to generate INTx interrupt s- Messages. When set, Functions devices are prevented from asserting generating INTx interrupt s- Messages.</p> <p>Any INTx emulation interrupts already asserted by the Function device must be deasserted when this bit is set.</p> <p><del>Note that INTx emulation interrupts forwarded by Root and Switch Ports from devices downstream of the Root or Switch Port are not affected by this bit.</del></p> <p><u>As described in Section 2.2.8.1, INTx interrupts use virtual wires that must, if asserted, be deasserted using the appropriate Deassert INTx message(s) when this bit is set.</u></p> <p><u>Only the INTx virtual wire interrupt(s) associated with the Function(s) for which this bit is set are affected.</u></p> <p><u>For Endpoints that generate INTx interrupts, this bit is required. For Endpoints that do not generate INTx interrupts this bit is optional. If not implemented, this bit must be hardwired to 0b.</u></p> <p><u>For Root Ports, Switch Ports and Bridges that generate INTx interrupts on their own behalf, this bit is required. This bit has no effect on interrupts that pass through the port from the secondary side.</u></p> <p><u>For Root Ports, Switch Ports and Bridges that do not generate INTx interrupts on their own behalf this bit is optional. If not implemented, this bit must be hardwired to 0b.</u></p> <p>Default value of this field is 0.</p>	RW

In Section 7.8.4, edit as shown:

7.8.4. Device Control Register (Offset 08h)

240 ...

Table 7-12: Device Control Register

Bit Location	Register Description	Attributes
...		
7:5	<p><b>Max_Payload_Size</b> – This field sets maximum TLP payload size for the device/function.</p> <p>...</p> <p>Default value of this field is 000b.</p> <p><u>Devices that support only the 128 byte max payload size are permitted to hardwire this field to 000b.</u></p> <p>System software is not required to program the same value for this field for all the functions of a multi-function device. See Section 2.2.2 for important guidance.</p>	RW
...		
14:12	<p><b>Max_Read_Request_Size</b> – This field sets the maximum Read Request size for the Device as a Requester.</p> <p>...</p> <p>Devices that do not generate Read Request larger than 128 bytes <u>and devices that do not generate read requests on their own behalf</u> are permitted to implement this field as Read Only (RO) with a value of 000b.</p> <p>Default value of this field is 010b.</p>	RW

*In Sections 7.8.6, 7.8.7, and 7.8.8 change as shown:*

### 7.8.6. Link Capabilities Register (Offset 0Ch)

245 ...

Table 7-14: Link Capabilities Register

Bit Location	Register Description	Attributes
3:0	<p><b>Maximum Link Speed</b> – ...</p> <p>All other encodings are reserved.</p> <p><u>Multi-function devices must report the same value in this field for all functions.</u></p>	RO
9:4	<p><b>Maximum Link Width</b> – ...</p> <p>100000b x32</p> <p><u>Multi-function devices must report the same value in this field for all functions.</u></p>	RO

Bit Location	Register Description	Attributes
11:10	<b>Active State Power Management (ASPM) Support – ...</b> <u>Multi-function devices must report the same value in this field for all functions.</u>	RO
14:12	<b>L0s Exit Latency – ...</b> ...component uses a common or separate reference clock. <u>Multi-function devices must report the same value in this field for all functions.</u>	RO
17:15	<b>L1 Exit Latency – ...</b> ... component uses a common or separate reference clock. <u>Multi-function devices must report the same value in this field for all functions.</u>	RO
18	<b>Clock Power Management – <u>For Upstream Ports, aA</u></b> value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) ... For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multi-function device indicate a 1b in this bit. <u>For Downstream Ports this bit must be hardwired to 0b.</u>	RO
19	<b>Surprise Down Error Reporting Capable – ...</b>	RO
20	<b>Data Link Layer Link Active Reporting Capable – ...</b>	RO
31:24	<b>Port Number –</b> This field indicates the PCI Express Port number for the given PCI Express Link. <u>Multi-function devices must report the same value in this field for all functions.</u>	HwInit

...

250 7.8.7. Link Control Register (Offset 10h)

...

Table 7-15: Link Control Register

Bit Location	Register Description	Attributes
--------------	----------------------	------------

Bit Location	Register Description	Attributes
1:0	<p><b>Active State Power Management (ASPM) Control</b> – This field controls the level of ASPM supported on the given PCI Express Link.</p> <p>...</p> <p><u>For multi-function devices, it is recommended that software program the same value for this field in all functions. Only capabilities enabled in all functions are enabled for the component as a whole.</u></p>	RW
3	<p>...</p> <p><i>Endpoints <u>and Bridges</u>:</i></p> <p><b>Read Completion Boundary (RCB)</b> – <del>Optionally May be</del> set by configuration software to indicate the RCB value of the Root Port upstream from the Endpoint. Refer to Section 2.3.1.1 for the definition of the parameter RCB.</p> <p>Defined encodings are:</p> <p>0b        64 byte</p> <p>1b        128 byte</p> <p><u>Configuration software must only set this bit to 1b if the Root Complex reports an RCB value of 128 bytes (a value of 1b in the Read Completion Boundary field).</u></p> <p><u>Default value of this field is 0b.</u></p> <p>Devices that do not implement this feature must hardwire the field to 0b.</p> <p>...</p>	<p>...</p> <p><i>Endpoints <u>and Bridges</u>:</i></p> <p>RW</p> <p>...</p>
4	<p><b>Link Disable</b> – This bit disables the Link <u>by directing the LTSSM to the Disabled state</u> when set to 1b; this field is <del>not applicable and</del> reserved <del>onfor</del> Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.</p> <p>...</p>	RW
5	<p><b>Retrain Link</b> – ...</p>	RW

Bit Location	Register Description	Attributes
6	<p><b>Common Clock Configuration</b> – This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.</p> <p>A value of 0b indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock.</p> <p><u>For multi-function devices, it is highly recommended that software program the same value for this field in all functions. If not all functions are set to 1b, then the component must as a whole assume that its reference clock is not common with the upstream component.</u></p> <p>Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.</p> <p>...</p>	RW
7	<p><b>Extended Synch</b> – This bit when set forces the transmission of additional ordered sets when exiting the L0s state (see Section 4.2.4.3) and when in the Recovery state (see Section 4.2.6.4.1). This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication.</p> <p><u>For multi-function devices if any function has this bit set to 1b, then the component must transmit the additional ordered sets when exiting L0s.</u></p> <p>Default value for this bit is 0b.</p>	RW



Bit Location	Register Description	Attributes
8	<p><b>Enable Clock Power Management</b> – Applicable only for <u>Upstream Ports and with</u> form factors that support a “Clock Request” (CLKREQ#) mechanism, this <u>bit operates enable-functions</u> as follows:</p> <p>0b – Clock power management is disabled and device must hold CLKREQ# signal low.</p> <p>1b - When this bit is set to 1, the device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification.</p> <p><u>For a multi-function device, power management configuration software is only permitted to set this bit to 1b if all functions of the multi-function device indicate a 1b in the Clock Power Management bit of the Link Capabilities Register. The component is permitted to use CLKREQ# signal to power manage link clock only if this bit is set for all functions.</u></p> <p>Default value of this field is 0b.</p> <p><u>For Downstream Ports and</u> Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities register) must hardwire this bit to 0b.</p>	RW

...

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### 7.8.8. Link Status Register (Offset 12h)

...

Table 7-16: Link Status Register

Bit Location	Register Description	Attributes
3:0	<b>Link Speed</b> – ...	RO
9:4	<b>Negotiated Link Width</b> – ...	RO
10	<b>Undefined</b> – ...	RO
11	<b>Link Training</b> – ...	RO
12	<p><b>Slot Clock Configuration</b> – This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear.</p> <p><u>For a multi-function device, each function must report the same value for this bit.</u></p>	Hwlnit
13	<b>Data Link Layer Link Active</b> – ...	RO

...

260 7.8.10. Slot Control Register (Offset 18h)

...

Table 7-18: Slot Control Register

<b>Bit Location</b>	<b>Register Description</b>	<b>Attributes</b>
0	<p><b>Attention Button Pressed Enable</b> – When set to 1b, this bit enables software notification on an attention button pressed event. See Section 6.7.3.</p> <p>Default value of this field is 0b. <u>If the Attention Button Present bit in the Slot Capabilities Register is 0b, this bit is permitted to be read-only with a value of 0b.</u></p>	RW
...		
3	<p><b>Presence Detect Changed Enable</b> – When set to 1b, this bit enables software notification on a presence detect changed event. See Section 6.7.3.</p> <p>Default value of this field is 0b. <u>If the Hot-Plug Capable bit in the Slot Capabilities Register is 0b, this bit is permitted to be read-only with a value of 0b.</u></p>	RW
...		
7:6	<p><b>Attention Indicator Control</b> – If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state.</p> <p>...</p> <p>Note: The default value of this field must be one of the non-Reserved values. <u>If the Attention Indicator Present bit in the Slot Capabilities Register is 0b, this bit is permitted to be read-only with a value of 00b.</u></p>	RW
9:8	<p><b>Power Indicator Control</b> – If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state.</p> <p>...</p> <p>Note: The default value of this field must be one of the non-Reserved values. <u>If the Power Indicator Present bit in the Slot Capabilities Register is 0b, this bit is permitted to be read-only with a value of 0b.</u></p>	RW
...		

Bit Location	Register Description	Attributes
12	<p><b>Data Link Layer State Changed Enable</b> – If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.</p> <p><u>If the Data Link Layer Link Active capability is not implemented, this bit is permitted to be read-only with a value of 0b.</u></p>	RW

265

---

## C16. Assorted

**PWG Approved 30 March 2006 -- Release Date: 8 May 2006**

*In Section 2.3, add:*

270 *Add in Terms and Acronyms:*

AER                    Advanced Error Reporting capability (see Section 7.10)

...

Transaction ID    A component of the Transaction Descriptor including the Requester ID and Tag

275 *Throughout the document, replace all instances of “Requestor ID” with “Requester ID”*

*In Section 2.2.2:*

- The size of the data payload of a Received TLP as given ~~be~~by the TLP’s Length [ ] ...

*In 4.2.4.4., edit as shown:*

280 **4.2.4.4. Link Error Recovery**

- Link Errors are defined as 8b/10b decode errors, loss of Symbol lock, Elasticity Buffer Overflow/Underflow, or loss of Lane-to-Lane de-skew.
  - Note: 8b/10b decode errors must be checked and trigger a Receiver Error in specified LTSSM states (see <>), which is a reported error associated with the Port (see Section <>). Triggering a Receiver Error on any or all of Framing Error, Loss of Symbol Lock, Lane Deskew Error, and Elasticity Buffer Overflow/Underflow is optional.

285

*In Section 4.2.6, Table 4-4., edit as shown:*

Table 4-4: Table of Link Status Mapped to the LTSSM

LTSSM State	Link Width	Link Speed	LinkUp	Link Training	Receiver Error	In-Band Presence <sup>2</sup> <sub>7</sub>
...						
Disabled	Undefined	Undefined	0	0	<u>Optional:</u> Set on 8b/10b Error	1
...						
Hot Reset	No Action	No Action	0	0	<u>Optional:</u> Set on 8b/10b Error	1

290

In Section 6.2.4:

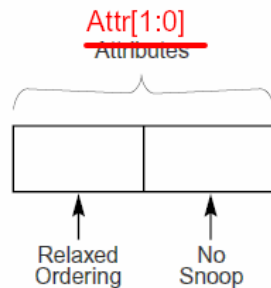
The following PCI Express errors are not function-specific:

- All Physical Layer errors
- All Data Link Layer errors
- These Transaction Layer errors:
  - ECRC Fail
  - UR, when caused by no function claiming a TLP
  - Receiver Overflow
  - Flow Control Protocol Error
  - Malformed TLP
  - Unexpected Completion

295

300

Modify Figure 2-12 as shown:



OM13759

**Figure 2-12: Attributes Field of Transaction Descriptor**

305

Section 5.3.3.2.:

Before using any wakeup mechanism, functions must be enabled by software to do so by setting the device's PME\_En bit in the Power Management Control/Status register (PMCSR). The PME\_Status bit is sticky, and devices must maintain the value of the PME\_Status bit through reset if aux power is available and they are enabled for wakeup events (this requirement also applies to the PME Enable bit in the PMCSR and the Aux Power PM Enable bit in the Device Control Register).

In Figure 7-70 Change:

"VAT\_Offset \* ~~04h~~10h" for VC Arbitration Table

"FAT\_Offset(0) \* ~~04h~~10h"

"FAT\_Offset(n) \* ~~04h~~10h" for Function Arbitration Table (0) and (n)

In Section 7.11.8, change:

1	<p><b>VC Negotiation Pending</b> –This bit indicates whether the Virtual Channel negotiation (initialization or disabling) is in pending state. This field is valid for all devices.</p> <p><u>The value of this field is defined only when the link is in the DL_Active state and the Virtual Channel is enabled (its VC Enable bit is set).</u></p> <p>When this bit is set by hardware, it indicates that the VC resource has not completed the process of negotiation. This bit is cleared by hardware after the VC negotiation is complete (on exit from the FC_INIT2 state). <u>For VC0, this bit is permitted to be hardwired to 0b.</u></p> <p>...</p>	RO
---	--	----

---

## C17. FC Advertisement Check Not Actually Possible

**PWG Approved 30 March 2006 -- Release Date: 8 May 2006**

In Section 2.6.1, edit as shown:

- During FC initialization for any Virtual Channel, including the default VC initialized as a part of Link initialization, Receivers must initially advertise VC credit values equal to or greater than those shown in Table 2 27.

330

~~• Components may optionally check for violations of this rule. If a component implementing this check determines a violation of this rule, the violation is a Flow Control Protocol Error (FCPE)~~

~~• If checked, this is a reported error associated with the Receiving Port (see Section 6.2)~~

335

---

## C18. AckNak\_LATENCY\_TIMER Clarifications

PWG Approved 30 March 2006 -- Release Date: 8 May 2006

Change the following text as shown:

### 3.5.3.1. LCRC and Sequence Number Rules (TLP Receiver)

...

340

The following timer is used:

~~• AckNak\_LATENCY\_TIMER – Counts time since an Ack or Nak DLLP was scheduled for transmission~~ Counts time that determines when an Ack DLLP becomes scheduled for transmission, according to the following rules:

345

- Set to 0 in DL\_Inactive state
- Restart from 0 each time an Ack or Nak DLLP is scheduled for transmission; Reset to 0 when all TLPs received have been acknowledged with an Ack DLLP
- If there are initially no unacknowledged TLPs and a TLP is then received, the AckNak\_LATENCY\_TIMER starts counting only when the TLP has been forwarded to the Receive Transaction Layer

350

...

~~An~~ A TLP Receiver must schedule an Ack DLLP ~~must be transmitted~~ such that it will be transmitted no later than when all of the following conditions are true:

355

- The Data Link Control and Management State Machine is in the DL\_Active state
- TLPs have been forwarded to the Receive Transaction Layer, but not yet acknowledged by sending an Ack DLLP
- The AckNak\_LATENCY\_TIMER reaches or exceeds the value specified in Table 3-5
- ~~The Link used for Ack DLLP transmission is already in L0 or has transitioned to L0~~  
Note: if not already in L0, the Link must transition to L0 in order to transmit the Ack DLLP
- Another TLP or DLLP is not currently being transmitted on the Link used for Ack DLLP transmission

360

- The NAK\_SCHEDULED flag is clear

Note: The AckNak\_LATENCY\_TIMER must be restarted from 0 each time an Ack or Nak DLLP is scheduled for transmission

- 365  Data Link Layer Ack DLLPs may be scheduled for transmission more frequently than required
- Data Link Layer Ack and Nak DLLPs specify the value (NEXT\_RCV\_SEQ - 1) in the AckNak\_Seq\_Num field

370 Table 3-5 defines the threshold values for the AckNak\_LATENCY\_TIMER ~~timer~~, which for any specific case is called the Ack Latency. The values are specified according to the largest TLP payload size and Link width. ~~The values are measured at the Port of the TLP Receiver, starting with the time the last Symbol of a TLP is received to the first Symbol of the Ack/Nak DLLP being transmitted.~~ The values are calculated using the formula:

$$\frac{(Max\_Payload\_Size + TLPOverhead) * AckFactor}{LinkWidth} + InternalDelay + Tx\_L0s\_Adjustment$$

375 where

Max\_Payload\_Size is the value in the Max\_Payload\_Size field of the Device Control register. For a multi-function device whose Max\_Payload\_Size settings are identical across all functions, the common Max\_Payload\_Size setting must be used. For a multi-function device whose Max\_Payload\_Size settings are not identical across all functions, the selected Max\_Payload\_Size setting is implementation specific, but it's recommended to use the smallest Max\_Payload\_Size setting across all functions.

380 TLP Overhead represents the additional TLP components which consume Link bandwidth (header, LCRC, framing Symbols) and is treated here as a constant value of 28 Symbols.

385 AckFactor represents the number of maximum size TLPs which can be received before an Ack is sent, and is used to balance Link bandwidth efficiency and retry buffer size – the value varies according to Max\_Payload\_Size and Link width, and is defined in Table 3-5.

390 LinkWidth is the operating width of the Link.

InternalDelay represents the internal processing delays for received TLPs and transmitted DLLPs, and is treated here as a constant value of 19 Symbol Times.

~~Tx\_L0s\_Adjustment if L0s is enabled, the time required for the Transmitter to exit L0s (see Section 4.2.6.6.2), expressed in Symbol Times, or 0 if L0s is not enabled.~~

395 ~~————— Note that the setting of the Extended Synch bit of the Link Control register affects the exit time from L0s to L0, and must be taken into account in this adjustment.~~

~~————— The values in Table 3-5 do not include this adjustment offset.~~

400 Thus, the Ack Latency is the value given in Table 3-5 plus the Transmitter L0s adjustment offset, described above.

TLP Receivers and compliance tests must base Ack Latency timing as measured at the Port of the TLP Receiver, starting with the time the last Symbol of a TLP is received to the first Symbol of the Ack DLLP being transmitted.

405 When measuring until the Ack DLLP is transmitted, compliance tests must allow for any TLP or  
 other DLLP transmission already in progress in that direction (thus preventing the Ack DLLP  
 transmission). If L0s is enabled, compliance tests must allow for the L0s exit latency of the Link  
 in the direction that the Ack DLLP is being transmitted. If the Extended Synch bit of the Link  
 Control register is set, compliance tests must also allow for its effect on L0s exit latency.

410 TLP Receivers are not required to adjust their Ack DLLP scheduling based upon L0s exit latency  
 or the value of the Extended Synch bit.

Table 3-5: *Unadjusted*<sup>†</sup> Ack Transmission Latency Limit and AckFactor by Link Width and Max Payload (Symbol Times)

		Link Operating Width						
		x1	x2	x4	x8	x12	x16	x32
<b>Max_Payload_Size (bytes)</b>	<b>128</b>	237 AF = 1.4	128 AF = 1.4	73 AF = 1.4	67 AF = 2.5	58 AF = 3.0	48 AF = 3.0	33 AF = 3.0
	<b>256</b>	416 AF = 1.4	217 AF = 1.4	118 AF = 1.4	107 AF = 2.5	90 AF = 3.0	72 AF = 3.0	45 AF = 3.0
	<b>512</b>	559 AF = 1.0	289 AF = 1.0	154 AF = 1.0	86 AF = 1.0	109 AF = 2.0	86 AF = 2.0	52 AF = 2.0
	<b>1024</b>	1071 AF = 1.0	545 AF = 1.0	282 AF = 1.0	150 AF = 1.0	194 AF = 2.0	150 AF = 2.0	84 AF = 2.0
	<b>2048</b>	2095 AF = 1.0	1057 AF = 1.0	538 AF = 1.0	278 AF = 1.0	365 AF = 2.0	278 AF = 2.0	148 AF = 2.0
	<b>4096</b>	4143 AF = 1.0	2081 AF = 1.0	1050 AF = 1.0	534 AF = 1.0	706 AF = 2.0	534 AF = 2.0	276 AF = 2.0

<sup>†</sup>The values in this table are determined using the formula shown above minus the “Tx\_L0s\_Adjustment” term.





## IMPLEMENTATION NOTE

### Retry Buffer Sizing

415 The Retry Buffer should be large enough to ensure that under normal operating conditions, transmission is never throttled because the retry buffer is full. In determining the optimal buffer size, one must consider the Ack Latency value, ~~any differences between the actual implementation and the internal processing delay used to generate these values~~ Ack delay caused by the Receiver already transmitting another TLP, ~~and~~ the delays caused by the physical Link interconnect, and the time required to process the received Ack DLLP.

420 ~~The Receiver's Transmitter L0s exit latency (see Section 4.6.2.2.1) should also be accounted for, as is demonstrated with the following example using components A and B: Given two components A and B, the L0s exit latency required by A's receiver should be accounted for when sizing A's transmit retry buffer, as is demonstrated in the following example:~~

- A exits L0s on its Transmit path to B and starts transmitting a long burst of write Requests to B
- 425  B initiates L0s exit on its Transmit path to A, but the L0s exit time required by A's Receiver is large
- Meanwhile, B is unable to send Ack DLLPs to A, and A stalls due to lack of Retry Buffer space
- The Transmit path from B to A returns to L0, B transmits an Ack DLLP to A, and the stall is resolved

430 This stall can be avoided by matching the size of a component's **Transmitter** Retry Buffer to the L0s exit latency ~~of required by~~ the component's Receiver, or, conversely, **by** matching the Receiver L0s exit latency to the desired size of the Retry Buffer.

435 AckFactor values were chosen to allow implementations to achieve good performance without requiring an uneconomically large retry buffer. To enable consistent performance across a general purpose interconnect with differing implementations and applications, it is necessary to set the same requirements for all components without regard to the application space of any specific component. If a component does not require the full transmission bandwidth of the Link, it may reduce the size of its retry buffer below the minimum size required to maintain available retry buffer space with the Ack Latency values specified.

440 Note that the Ack Latency values specified ensure that the range of permitted outstanding Sequence Numbers will never be the limiting factor causing transmission stalls.

---

## C19. Assorted

445 PWG Approved 30 March 2006 -- Release Date: 8 May 2006

*In Section 5.4.1.2.1, edit as shown:*

450 The Upstream component sends this DLLP repeatedly with no more than 4 symbol times of idle between subsequent transmissions of the PM\_Request\_Ack DLLP. The transmission of SKP ordered sets ~~is~~ **must occur as required** at any time between PM\_Request\_Ack transmissions, and do not contribute to the 4 symbol time idle limit. Transmission of SKP ordered sets during L1 entry follows the clock tolerance compensation rules in section 4.2.7

*In Section 3.5.2, insert a new subsection header as shown:*

**3.5.2.2. Handling of Received DLLPs**

455  Since Ack/Nak and Flow Control DLLPs affect TLPs flowing in the opposite direction across the Link, the TLP transmission mechanisms in the Data Link Layer are also responsible for Ack/Nak and Flow Control DLLPs received from the other component on the Link. ...

*In Section 2.2.8 delete as shown:*

460 ...

~~Hot-Plug Signaling~~

*In Section 2.2.8.7 edit as shown:*

465 The messages listed in Table 2-19 were previously used for a mechanism (Hot-Plug Signaling) that is no longer supported.

*In Section 2.9.1, edit as shown:*

**2.9.1 Transaction Layer Behavior in DL\_Down Status**

...

470  The Port must terminate any PME Turn Off handshake Requests targeting the port in such a way that the port is considered to have acknowledged the PME Turn Off request (see Implementation Note in Section 5.3.3.2.1)

for all other Posted Requests, discarding the Requests

...

---

475 **C20. REPLAY\_TIMER Clarifications**

**PWG Approved 30 March 2006 – Release Date: 8 May 2006**

*Change the following text as shown:*

**3.5.2.1. LCRC and Sequence Number Rules (TLP Transmitter)**

...

- 480  The following timer is used:
- **REPLAY\_TIMER** - ~~Counts time since last Ack or Nak DLLP received~~ Counts time that determines when a replay is required, according to the following rules:
    - ◆ Started at the last Symbol of any TLP transmission or retransmission, if not already running
    - 485 ◆ For each replay, reset and restart REPLAY\_TIMER when sending the last Symbol of the first TLP to be retransmitted
    - ◆ Restarts for each Ack DLLP received while there are unacknowledged TLPs outstanding, if, and only if, the received Ack DLLP acknowledges some TLP in the retry buffer
    - 490 ■ **Note:** This ensures that REPLAY\_TIMER is reset only when forward progress is being made
    - ◆ Reset and hold until restart conditions are met for each Nak received (except during a replay) or when the REPLAY\_TIMER expires
    - ◆ Not advanced during Link retraining (holds its value when the LTSSM is in the Recovery or Configuration state). See Sections 4.2.5.3 and 4.2.5.4.
    - 495 ◆ Resets and holds when there are no outstanding unacknowledged TLPs

...

When a replay is initiated, either due to reception of a Nak or due to REPLAY\_TIMER expiration, the following rules describe the sequence of operations that must be followed:

- 500  If all TLPs transmitted have been acknowledged (the Retry Buffer is empty), terminate replay, otherwise continue.
- Increment REPLAY\_NUM.
- If REPLAY\_NUM rolls over from 11b to 00b, the Transmitter signals the Physical Layer to retrain the Link, and waits for the completion of retraining before proceeding with the replay. This is a reported error associated with the Port (see Section 6.2).

Note that Data Link Layer state, including the contents of the Retry Buffer, are not reset by this action unless the Physical Layer reports Physical LinkUp = 0 (causing the Data Link Control and Management State Machine to transition to the DL\_Inactive state).

- 510 • If REPLAY\_NUM does not roll over from 11b to 00b, continue with the replay.
- Block acceptance of new TLPs from the Transmit Transaction Layer.

...

The following formula defines the timeout count values for the REPLAY\_TIMER. The values are specified according to the largest TLP payload size and Link width.

515 ~~The values are measured at the Port of the TLP Transmitter, from last Symbol of TLP to First Symbol of TLP retransmission.~~ The values are calculated using the formula (note – this is simply three times the Ack Latency value – see Section 3.5.3.1):

$$\left( \frac{(\text{Max\_Payload\_Size} + \text{TLPOverhead}) * \text{AckFactor}}{\text{LinkWidth}} + \text{InternalDelay} \right) * 3 + \text{Rx\_L0s\_Adjustment}$$

520 where

Max\_Payload\_Size is the value in the Max\_Payload\_Size field of the Device Control register. For a multi-function device whose Max\_Payload\_Size settings are identical across all functions, the common Max\_Payload\_Size setting must be used. For a multi-function device whose Max\_Payload\_Size settings are not identical across all functions, the selected Max\_Payload\_Size setting is implementation specific, but it's recommended to use the largest Max\_Payload\_Size setting across all functions.

525

TLP Overhead represents the additional TLP components which consume Link bandwidth (header, LCRC, framing Symbols) and is treated here as a constant value of 28 Symbols

530

AckFactor represents the number of maximum size TLPs which can be received before an Ack is sent, and is used to balance Link bandwidth efficiency and retry buffer size – the value varies according to Max\_Payload\_Size and Link width, and is included in Table 3-5

535

LinkWidth is the operating width of the Link

InternalDelay represents the internal processing delays for received TLPs and transmitted DLLPs, and is treated here as a constant value of 19 Symbol Times

540 ~~Rx\_L0s\_Adjustment equals the time required by the component's receive circuits to exit from L0s to L0 (as to receive an Ack DLLP from the other component on the Link) expressed in Symbol Times (see Section 4.2.6.6.1)~~

~~\_\_\_\_\_ The values in Table 3-4 do not include this adjustment offset.~~

~~Thus, the timeout value for REPLAY\_TIMER is the value given in Table 3-4 plus the Receiver-L0s adjustment offset, described above.~~

545 ~~TLP Transmitters and compliance tests must base replay timing as measured at the Port of the TLP Transmitter. Timing starts with either the last Symbol of a transmitted TLP, or else the last Symbol of a received Ack DLLP, whichever determines the oldest unacknowledged TLP. Timing ends with the First Symbol of TLP retransmission.~~

550 ~~It is strongly recommended that a TLP Transmitter not perform a TLP retransmission due to Ack delay if the delay is potentially caused by the Ack's Link needing to exit L0s before it can transmit the Ack. This might be accomplished by statically adjusting the REPLAY\_TIMER to allow for the L0s exit latency of the Ack's Link, or by sensing if the Ack's Link is in the process of exiting L0s when the REPLAY\_TIMER expires.~~

555

When measuring replay timing to the point when TLP retransmission begins, compliance tests must allow for any other TLP or DLLP transmission already in progress in that direction (thus preventing the TLP retransmission). Also, if either Link is enabled for L0s, compliance tests must allow for L0s exit latency<sup>2</sup>, either with the Link over which the Ack is transmitted, or with the Link over which the TLP is retransmitted.

**Table 3-4: Unadjusted<sup>3</sup> REPLAY\_TIMER Limits by Link Width and Max\_Payload\_Size (Symbol Times)  
Tolerance: -0%/+100%**

		Link Operating Width						
		x1	x2	x4	x8	x12	x16	x32
Max_Pa yload_ Size (bytes)	128	711	384	219	201	174	144	99
	256	1248	651	354	321	270	216	135
	512	1677	867	462	258	327	258	156
	1024	3213	1635	846	450	582	450	252
	2048	6285	3171	1614	834	1095	834	444
	4096	12429	6243	3150	1602	2118	1602	828

<sup>2</sup> Note that L0s exit latency is affected by the value of the Extended Synch bit in the Link Control register.

<sup>3</sup> ~~The values in this table are determined using the formula shown above minus the “Rx\_L0s\_Adjustment” term.~~ A TLP Transmitter is permitted to adjust its REPLAY\_TIMER to allow for L0s exit latency as described in the text preceding the table.

560

---

## C21. Text Updates for Trusted Configuration

PWG Approved 15 June 2006 – Release Date: 25 August 2006

*Note: This errata builds on the Trusted Configuration ECN (already approved & released)*

*Change In Section 2.2.6.4 Relaxed Ordering Attribute:*

565 This attribute is not applicable and must be set to 0b for Configuration Rrequests, Trusted Configuration Rrequests, I/O Rrequests, Memory Rrequests that are Message Signaled Interrupts, and Message Rrequests (except where specifically permitted).

*Change In Section 2.2.6.5 No Snoop Attribute:*

570 This attribute is not applicable and must be set to 0b for Configuration Rrequests, Trusted Configuration Rrequests, I/O Rrequests, Memory Rrequests that are Message Signaled Interrupts, and Message Rrequests (except where specifically permitted).

*In the Trusted Configuration ECN Section 7.21.3.2:*

... Software must qualify the VSTCVTSC Vendor ID ...

575

---

## C22. L1 Invocation Example

PWG Approved 15 June 2006 – Release Date: 25 August 2006

*In the implementation note in section 5.4.1.2.1 change:*

580 One possible approach would be for the Downstream device to initiate a transition to the L1 state once the device has both its Receiver and Transmitter in the L0s state (RxL0s and TxL0s) for a set amount of time. Another approach would be for the Downstream device to initiate a transition to the L1 state once the link has been idle in L0 for a set amount of time. This is particularly useful if L0s entry is not enabled. Still another would be for the Downstream device to initiate a transition to the L1 state if it has completed its assigned tasks. Note that a component's L1 invocation policy is in no way limited by these few  
585 examples.

---

## C23. L1, L23\_Ready Negotiation

PWG Approved 15 June 2006 – Release Date: 25 August 2006

*Add an arc to Fig 5-1:*

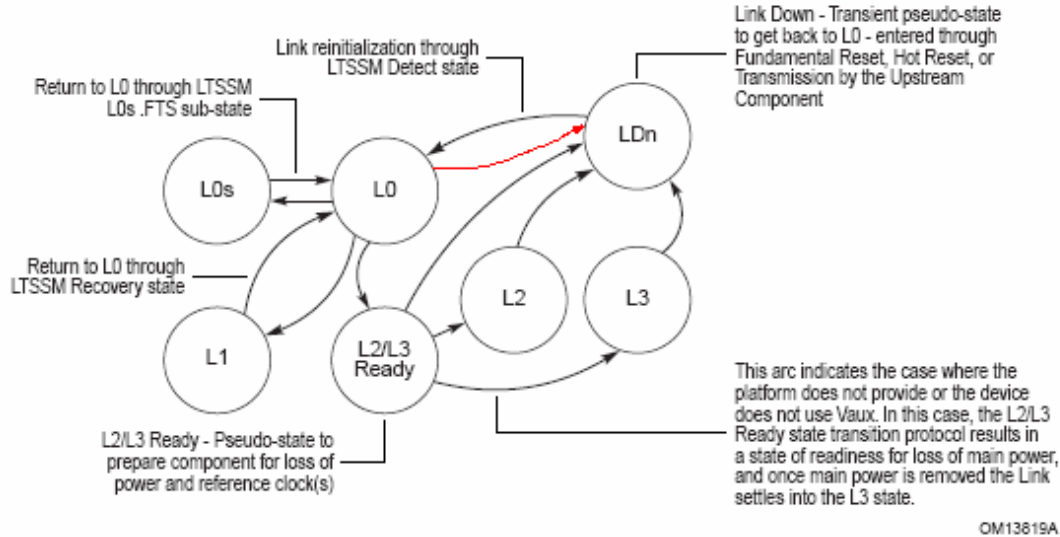


Figure 5-15-4: Link Power Management State Flow Diagram

590 IN ADDITION TO ARC ADDED IN THE FIGURE ABOVE change the upper right hand text in the figure as shown here:

... also entered through Fundamental Reset, Hot Reset, or Link Disable ~~T~~transmission by the ...

In section 5.2, after fig 5-1 and the two examples, but before the paragraph describing Table 5-1, add:

595 The L1 entry negotiation (whether invoked via PCI-PM or ASPM mechanisms) and the L2/L3 Ready entry negotiation map to a state machine which corresponds to the actions described later in this chapter. This state machine is reset to an idle state. For a downstream component, the first action taken by the state machine, after leaving the idle state, is to start sending the appropriate entry DLLPs depending on the type of negotiation. If the negotiation is interrupted, for example by a trip through Recovery, the state machine in both components is reset back to the idle state. For the upstream component, this always means to go to the idle state, and wait to receive entry DLLPs. For the downstream component, this means go to the idle state and proceed to sending entry DLLPs to restart the negotiation.

600

In section 5.2, expand the first sentence after fig 5-1:

605 The L1 and L23 Ready entry negotiations happen while in the L0 state. L1 and L23 Ready are entered only after the negotiation completes. Link Power Management remains in L0 until the negotiation process is completed, unless LDn occurs. Note that these states and state transitions do not correspond directly to the actions of the Physical Layer LTSSM. For example in Fig 5-1, L0 encompasses the LTSSM L0, Recovery, and during LinkUp, Configuration states. Also the LTSSM is typically powered by main power (not Vaux), and so in both the L2 and L3 states will be unpowered.

610 At the end of section 5.3.2.1, after item 10, add:

Refer to Section 5.2 if the negotiation to L1 is interrupted.

Components on either end of a Link in L1 may optionally disable their internal PLLs ...

At the end of section 5.3.2.3, add another major bullet:

- 615
- ❑ L2/L3 Ready entry transition protocol uses the PM\_Enter\_L23 DLLP. Note that the PM\_Enter\_L23 DLLPs are sent continuously until an acknowledgement is received or power is removed.
  - ❑ [Refer to section 5.2 if the negotiation to L2/L3 Ready is interrupted.](#)

*In section 5.4.1.2.1, at the end of the ASPM L1 Negotiation Rules, add another major bullet:*

- 620
- ❑ The Upstream component must immediately respond to the request with either an acceptance or a rejection of the request.
    - If the Upstream component is not able to accept the request, it must immediately reject the request.
  - ❑ [Refer to section 5.2 if the negotiation to L1 is interrupted.](#)
- 625

*In section 5.4.1.2.1, expand the minor bullet of the 2<sup>nd</sup> major bullet of the ASPM L1 Negotiation Rules as follows:*

If any TLPs become available from the Transaction Layer for transmission during the L1 negotiation process, the transition to L1 must first be completed and then the Downstream component must initiate a return to L0. [Refer to section 5.2 if the negotiation to L1 is interrupted.](#)

630 *In section 5.4.1.2.1, expand the 2<sup>nd</sup> minor bullet of the 5<sup>th</sup> major bullet of the ASPM L1 Negotiation Rules as follows:*

If the Downstream component for any reason needs to transmit a TLP on the Link, it must first complete the transition to the low power Link state. Once in a lower power Link state, the Downstream component must then initiate exit of the low power Link state to handle the transfer. [Refer to section 5.2 if the negotiation to L1 is interrupted.](#)

635

*In section 5.4.1.2.1, expand the 5<sup>th</sup> major bullet of the “Rules in case of acceptance” as follows:*

If the Upstream component needs, for any reason, to transmit a TLP on the Link after it sends a PM\_Request\_Ack DLLP, it must first complete the transition to the low power state, and then initiate an exit from the low power state to handle the transfer once the Link is back to L0. [Refer to section 5.2 if the negotiation to L1 is interrupted.](#)

640

---

## ***C24. Retrain Link Bit Only Exists for Upstream Components***

**PWG Approved 29 June 2006 – Release Date: 25 August 2006**

*In Section 5.4.1.3.1., change:*

645 PCI Express software updates the Common Clock Configuration bits in the components on both ends of each Link to indicate if those devices share the same reference clock and triggers Link retraining by writing 1 to the Retrain Link bit in the Link Control register of ~~one of~~ the [Upstream Components](#).

---

## ***C25. Definition of Completer***

**PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007**

*Change the following text as shown:*

650 **Terms and Acronyms**



...

Completer ~~The logical device addressed by a Request.~~ The Function that terminates or “completes” a given Request, and generates a Completion if appropriate. Generally the Function targeted by the Request serves as the Completer. For cases when an uncorrectable error prevents the Request from reaching its targeted Function, the Function that detects and handles the error serves as the Completer.

...

---

## C26. ECRC Rules

PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007

655 *Change the following text as shown:*

### 2.2.3. TLP Digest Rules

...

If ~~the device at the ultimate~~ an intermediate or ~~destination~~ ultimate PCI Express Receiver of the TLP does not support ECRC checking, the ~~device~~ Receiver must ignore the TLP Digest

660 If the ~~device at the ultimate destination~~ Receiver of the TLP supports ECRC checking, the ~~device~~ Receiver interprets the value in the TLP Digest field as an ECRC value, according to the rules in Section 2.7.1

### 2.7. Data Integrity

... To ensure end-to-end data integrity detection in systems that require high data reliability, a Transaction Layer end-to-end 32-bit CRC (ECRC) can be placed in the TLP Digest field at the end of a TLP. The ECRC covers all fields that do not change as the TLP traverses the path (invariant fields). The ECRC is generated by the Transaction Layer in the source component, and checked (if supported) ~~in by the destination component~~ ultimate PCI Express Receiver and optionally by intermediate Receivers. A Switch that supports ECRC checking ~~checks~~ must check ECRC on TLPs ~~that are destined to a destination within~~ targeting the Switch itself. Such a Switch can optionally check ECRC on TLPs that it forwards. On ~~all other~~ TLPs ~~a that the Switch forwards,~~ the Switch must preserve the ECRC (forward it untouched) as an integral part of the TLP, ~~regardless of whether the Switch checks the ECRC or if the ECRC check fails.~~

#### 2.7.1. ECRC Rules

...

Switches must pass TLPs with ECRC unchanged from the Ingress Port to the Egress Port

675 ~~If a device reports the capability to check ECRC, it must support~~ If a device supports ECRC generation/checking, at least one of its Functions must support Advanced Error Reporting (see Section 6.2)

If a device is enabled to check ECRC, it must do so for all TLPs ~~received by the device including~~ ECRC with ECRC where the device is the ultimate PCI Express Receiver

680 Note that it is still possible for the device to receive TLPs without ECRC, and these are processed normally – this is not an error

Note that a Switch may optionally perform ECRC checking on TLPs passing through the Switch. ECRC Errors detected by the Switch are reported as described in Table 6-4, but do not alter the TLPs’ passage through the Switch.

...

685 Receivers which support end-to-end data integrity checks report violations as an ECRC Error. This reported error is associated with the receiving port (see Section 6.2).

How ~~the Receiver makes~~ ultimate PCI Express Receivers make use of the end-to-end data integrity check provided through the ECRC is beyond the scope of this document. ~~Intermediate Receivers are still required to forward TLPs whose ECRC checks fail. A PCI Express-to-PCI/PCI-X Bridge is classified as an ultimate PCI Express Receiver with regard to ECRC checking.~~

---

690 **C27. Redundant Example in Section 2.2.6.2.**

**PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007**

*Change the following text as shown:*

**2.2.6.2. Transaction Descriptor – Transaction ID Field**

...

695 Functions must capture the Bus and Device Numbers supplied with all Configuration Write Requests (Type 0) completed by the function and supply these numbers in the Bus and Device Number fields of the Requester ID for all Requests initiated by the device/function.

Exception: The assignment of Bus and Device Numbers to the logical devices within a Root Complex, and Device Numbers to the downstream ports within a switch, may be done in an implementation specific way.

700 Note that the Bus Number and Device Number may be changed at run time, and so it is necessary to re-capture this information with each and every Configuration Write Request.

705 ~~Example: When a device (or function of a multi-function device) receives a Type 0 Configuration Write Request, the device comprehends that it is the intended recipient of the Request because it is a Type 0 Request. The routing information fields of the Write Request include the recipient's Bus Number and Device Number values (Figure 2-16). These values are captured by the device and used to generate the Requester and Completer ID field.~~

---

**C28. Scope of TC Service Policy**

**PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007**

*Change the following text as shown:*

710 **2.2.6.6. Transaction Descriptor – Traffic Class Field**

...

The concept of Traffic Class applies only within the PCI Express interconnect fabric. Specific requirements of how PCI Express TC service policies are translated into policies on non-PCI Express interconnects ~~or within Root Complex or Endpoints~~ is outside of the scope of this specification.

715

---

**C29. PM Messages and BDF/BD**

**PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007**

*Change the following text as shown:*

**2.2.8.2. Power Management Messages**

720 ...

Table 2-14: Power Management Messages

Name	Code[7:0]	Routing r[2:0]	Support				Req ID	Description/Comments
			R C	E p	S w	B r		
PM_Active_State_Nak	0001 0100	100	t	r	tr	r	BDF <sup>1</sup>	Terminate at Receiver
PM_PME	0001 1000	000	All:				BDF	Sent Upstream by PME-requesting component. Propagates Upstream.
			r		tr	t		
			If PME supported:					
			t					
PME_Turn_Off	0001 1001	011	t	r		r	BDF	Broadcast Downstream
PME_TO_Ack	0001 1011	101	r	t		t	BDF <sup>2</sup>	Sent Upstream by- <del>Endpoint Upstream Port.</del> <del>Sent Upstream by Switch</del> <del>when received on all</del> <del>Downstream Ports.</del> See Section 5.3.3.2.1.
			(Note: Switch handling is special)					

<sup>1</sup> Also permitted to be BD for compatibility with earlier revisions of this specification.

<sup>2</sup> Also permitted to be BDF for compatibility with earlier revisions of this specification.

**5.6. Power Management System Messages and DLLPs**

725 ...

Power management Messages follow the general rules for PCI Express system Messages. Message fields follow the following rules:

Length field is reserved.

Attribute field must be set to the default values (all 0's).

730 Address field is reserved.

Requester ID - see Table 2-14 in Section 2.2.8.2.

**PM\_PME Message**

~~Endpoints report their Upstream Link bus number and the device and function number where the PME originated.~~

735 ~~All other devices report their Upstream Link bus and device numbers, and the function number must be zero.~~

Traffic Class field must use the default class (TC0).

---

**C30. VC Capability Is Indeed Optional**

**PWG Approved 19 Oct 2006 – Release Date: 8 Feb 2007**

Change the following text as shown:

740 **7.11. Virtual Channel Capability**

The PCI Express Virtual Channel (VC) capability is an optional extended capability that ~~is required to~~ can be implemented by PCI Express Ports of devices ~~that~~ to support PCI Express functionality beyond the general purpose I/O traffic, i.e., the default Traffic Class 0 (TC0) over the default Virtual Channel 0 (VC0). ...

---

### **C31. INTx Interrupt Status Clarification**

745 PWG Approved 14 Dec 2006 -- Release Date: 8 Feb 2007

*In Table 7-4: Status Register, Change:*

Bit Location	Register Description	Attributes
3	<b>Interrupt Status</b> – When Set, indicates that an INTx <u>emulation</u> interrupt <del>Message</del> is pending internally to the Function.  Note that INTx emulation interrupts forwarded by Root and Switch Ports from devices downstream of the Root or Switch Port are not reflected in this bit.  Default value of this bit is 0b.	RO
...		

---

### **C32. Reserved Fields in “2” Registers**

PWG Approved 14 Dec 2006 -- Release Date: 8 Feb 2007

750 *This Errata applies to the 1.1 + the Register Expansion ECN*

*Add text as shown below:*

#### 7.8.17. Device Status 2 Register (Offset 2Ah)

This section is a placeholder. There are no capabilities that require this register.

[This register must be treated by software as RsvdZ.](#)

755 7.8.18. Link Capabilities 2 Register (Offset 2Ch)

This section is a placeholder. There are no capabilities that require this register.

[This register must be treated by software as RsvdP.](#)

...

#### 7.8.21. Slot Capabilities 2 Register (Offset 34h)

760 This section is a placeholder. There are no capabilities that require this register.

[This register must be treated by software as RsvdP.](#)

#### 7.8.22. Slot Control 2 Register (Offset 38h)

This section is a placeholder. There are no capabilities that require this register.

This register must be treated by software as RsvdP.

765 7.8.23. Slot Status 2 Register (Offset 3Ah)

This section is a placeholder. There are no capabilities that require this register.

This register must be treated by software as RsvdZ.

---

**C33. Device Status Register Error Detected Bit Typos**

PWG Approved 14 Dec 2006 -- Release Date: 8 Feb 2007

770 7.8.5. Device Status Register (Offset 0Ah)

...

Bit Location	Register Description	Attributes
0	<p><b>Correctable Error Detected</b> – ...</p> <p>For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the <b>C</b>orrectable <b>E</b>rror <b>M</b>ask register.</p> <p>...</p>	RW1C
1	<p><b>Non-Fatal Error Detected</b> – ...</p> <p>For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the <b>U</b>ncorrectable <b>E</b>rror <b>M</b>ask register.</p> <p>...</p>	RW1C
2	<p><b>Fatal Error Detected</b> – ...</p> <p>For Functions supporting Advanced Error Handling, errors are logged in this register regardless of the settings of the <b>U</b>ncorrectable <b>E</b>rror <b>M</b>ask register.</p> <p>Default value of this bit is 0b.</p>	RW1C
...		

---

**C34. D0active**

PWG Approved 14 Dec 2006 -- Release Date: 8 Feb 2007

775 *In 5.3.1.4.1:*

Functions that are in D3<sub>hot</sub> may be transitioned by software (writing to their PMCSR PowerState

field) to the D0~~active~~initialized ...

---

### **C35. Assorted**

780 **PWG Approved 30 Nov 2006 -- Release Date: 8 Feb 2007**

*Note: There were discussed piecemeal and approved as a bunch in the PWG meeting 30 Nov 2006*

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#### 6.1.1.8. Operating System Power Management Notification

785 In order to maintain compatibility with non-PCI Express-aware system software, system power management logic must be configured by firmware to use the legacy mechanism of signaling PME by default. PCI Express-aware system software must notify the firmware prior to enabling native, interrupt-based PME signaling.

790 In response to this notification, system firmware must, if needed, reconfigure the Root Complex to disable legacy mechanisms of signaling PME. The details of this firmware notification are beyond the scope of this specification, but since it will be executed at system run-time, the response to this notification

795 must not interfere with system software. ~~Therefore, the firmware must not write to system available memory or I/O, or the Configuration Space headers of any PCI device Function.~~

Therefore, following control handoff to the operating system, firmware must not write to available system memory or any PCI Express resources (e.g., Configuration Space structures) owned by the operating system.

800

-----

**Status reg:**

805 **Signaled Target Abort – See Section 7.5.1.7.**

This bit is Set when a Function completes a Posted or Non-Posted Request using as a Completer Abort ~~Completion Status error~~. This applies to a Function with a Type 1 Configuration header when the Completer Abort was generated by its Primary Side.

810            **Secondary Status reg:**

**Signaled Target Abort** – See Section 7.5.1.7.

This bit is Set when the Secondary Side for Type 1 Configuration Space header Function (for Requests completed by the Type 1 header Function itself) completes a Posted or Non-Posted Request using as a Completer Abort ~~Completion Status error~~.

815

**6.x.4. ACS Violation Error Handling:**

...

When an ACS Violation is detected, the ACS component that operates as the Completer<sup>63</sup> must do the following:

820            For Non-Posted Requests, the Completer must generate a Completion with a Completer Abort (CA) Completion Status.

The Completer must log and signal the ACS Violation as indicated in Figure 6-2. Note the following:

- 825            • Even though the Completer uses a CA Completion Status when it sends a Completion, the Completer must log an ACS Violation error instead of a Completer Abort error.
- If the severity of the ACS Violation is non-fatal and the Completer sends a Completion with CA Completion Status, this case must be handled as an Advisory Non-Fatal Error as described in Section 6.2.3.2.4.1.
- 830            • The Completer<sup>64</sup> must set the Signaled Target Abort bit in either its Status register or Secondary Status register as appropriate.

835            <sup>64</sup> Similarly, if the Request was Non-Posted, when the Requester receives the resulting Completion with CA Completion Status, the Requester must set the Received Target Abort bit in either its Status register or Secondary Status register as appropriate. Note that for the case of a multi-Function device incurring an ACS Violation error with a peer-to-peer Request between its Functions, the same Function might serve both as Requester and Completer.

-----  
*Section 7.11.7, p. 555, VC Enable bit description:*

**VC Enable - ...**

840            Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. ~~When VC Negotiation Pending bit is cleared, a 1b read from this VC Enable bit indicates that the VC is enabled (Flow Control initialization is~~

~~completed for the PCI Express Port); a 0b read from this bit  
indicates that the Virtual Channel is currently disabled.~~

845 ...

-----  
**PCIe Cap reg:**

**Device/Port Type** – Indicates the specific type of this PCI Express Function. Note that different Functions in a multi-Function device can generally be of different types.

850 Defined encodings are:

0000b PCI Express Endpoint

0001b Legacy PCI Express Endpoint

0100b Root Port of PCI Express Root Complex\*

0101b Upstream Port of PCI Express Switch\*

855 0110b Downstream Port of PCI Express Switch\*

0111b PCI Express-to-PCI/PCI-X Bridge\*

1000b PCI/PCI-X to PCI Express Bridge\*

1001b Root Complex Integrated Endpoint

1010b Root Complex Event Collector

860 \*This value is only valid for Functions that implement a Type 01h PCI Configuration Space header.

All other encodings are reserved.

865 ~~Native PCI Express Endpoints that do not require I/O resources for correct operation indicate a Device/Port Type of 0000b; such Endpoints are permitted to request I/O resources (through BARs) for legacy boot support but system software is allowed to close requested I/O resources once appropriate services are made available to device specific software for access to device specific resources claimed through memory BARs.~~

~~Legacy PCI Express Endpoints that require I/O resources claimed through BARs for run-time operations indicate a Device Type of 0001b.~~

870 ~~Extended Configuration Space Capabilities, if implemented on legacy PCI Express Endpoints, are permitted to be ignored by software.~~

~~Note that the different Endpoint types have notably different requirements in Section 1.3.2. regarding I/O resources, Extended Configuration Space, and other capabilities.~~



875

***C36. Unexpected Completion Sometimes Function-Specific***

**PWG Approved 8 Feb 2007 -- Release Date: 8 Feb 2007**

*In 6.2.4. Error Logging:*

The following PCI Express errors are not Function-specific:

...

880

- Unexpected Completion, when caused by no Function claiming a Completion

---- end of errata ----