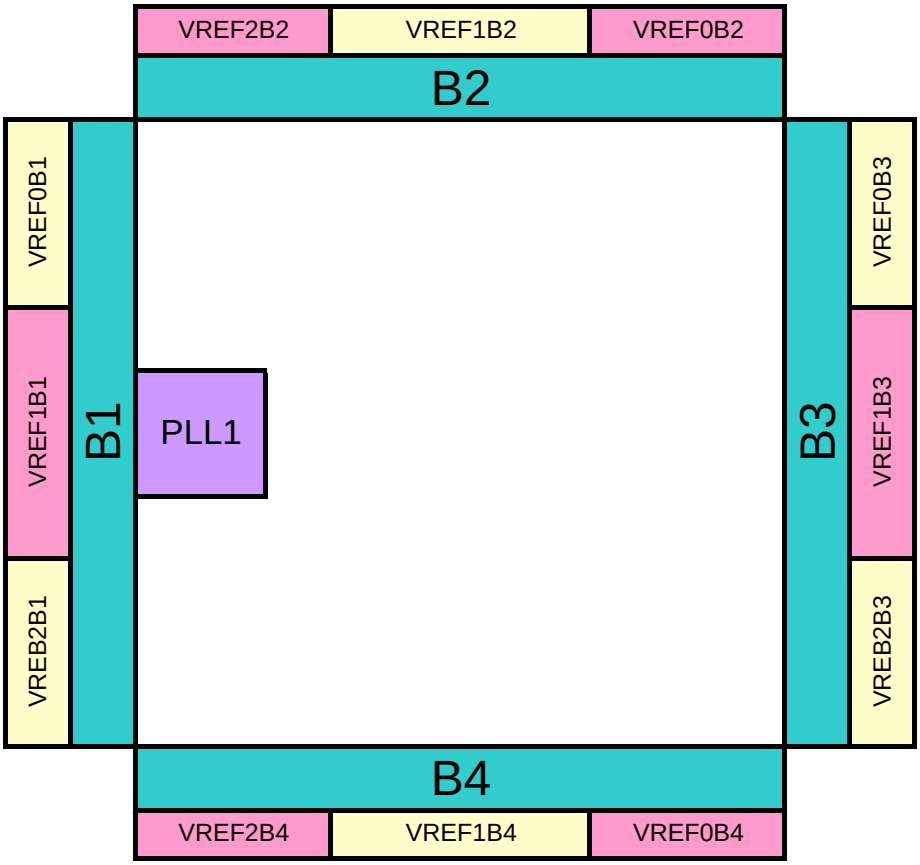
Pin Information for the Cyclone™ EP1C3T100 Device
Version 1.5

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T100	DQS for x8 in the T100
B1	VREF0B1	IO		INIT_DONE	1	
B1	VREF0B1	IO		CRC_ERROR	2	
B1	VREF0B1	IO		CLKUSR	3	
B1	VREF0B1	IO	VREF0B1		4	
B1	VREF0B1	VCCIO1				
B1	VREF0B1	GND				
B1	VREF1B1	IO	VREF1B1		5	
B1	VREF1B1	IO		nCSO	6	
B1	VREF1B1	DATA0		DATA0	7	
B1	VREF1B1	nCONFIG		nCONFIG	8	
	VREF1B1	VCCA_PLL1			9	
B1	VREF1B1	CLK0			10	
	VREF1B1	GNDA_PLL1			11	
B1	VREF1B1	nCEO		nCEO	12	
B1	VREF1B1	nCE		nCE	13	
B1	VREF1B1	MSEL0		MSEL0	14	
B1	VREF1B1	MSEL1		MSEL1	15	
B1	VREF1B1	DCLK		DCLK	16	
B1	VREF1B1	IO		ASDO	17	
B1	VREF2B1	VCCIO1			18	
B1	VREF2B1	GND			19	
B1	VREF2B1	IO	VREF2B1		20	
B1	VREF2B1	IO			21	
B1	VREF2B1	IO			22	
B1	VREF2B1	IO			23	
B1	VREF2B1	IO			24	
B1	VREF2B1	IO			25	
B4	VREF2B4	IO			26	
B4	VREF2B4	IO			27	DQ1B7
B4	VREF2B4	IO			28	DQ1B6
B4	VREF2B4	IO			29	DQ1B5
B4	VREF2B4	GND			30	
B4	VREF2B4	VCCIO4			31	
	VREF2B4	GND			32	
	VREF2B4	VCCINT			33	
B4	VREF2B4	IO	DPCLK7		34	DQS1B
B4	VREF2B4	IO	VREF2B4		35	
B4	VREF2B4	IO			36	DQ1B4
B4	VREF1B4	IO			37	
B4	VREF1B4	IO	VREF1B4		38	
B4	VREF1B4	IO			39	DM1B
B4	VREF1B4	IO			40	
B4	VREF0B4	IO	VREF0B4		41	
B4	VREF0B4	IO	DPCLK6		42	DQS0B
	VREF0B4	GND			43	
	VREF0B4	VCCINT			44	
B4	VREF0B4	GND			45	
B4	VREF0B4	VCCIO4			46	
B4	VREF0B4	IO			47	DQ1B3
B4	VREF0B4	IO			48	DQ1B2
B4	VREF0B4	IO			49	DQ1B1
B4	VREF0B4	IO			50	DQ1B0
B3	VREF2B3	IO			51	
B3	VREF2B3	IO			52	
B3	VREF2B3	IO			53	DQ0R7
B3	VREF2B3	IO			54	DQ0R6

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	T100	DQS for x8 in the T100
B3	VREF2B3	IO			55	DQ0R5
B3	VREF2B3	IO			56	DQ0R4
B3	VREF2B3	IO	VREF2B3		57	
B3	VREF2B3	GND			58	
B3	VREF2B3	VCCIO3			59	
B3	VREF1B3	CONF_DONE		CONF_DONE	60	
B3	VREF1B3	nSTATUS		nSTATUS	61	
B3	VREF1B3	TCK		TCK	62	
B3	VREF1B3	TMS		TMS	63	
B3	VREF1B3	TDO		TDO	64	
B3	VREF1B3	IO			65	DM0R
B3	VREF1B3	CLK2			66	
B3	VREF1B3	TDI		TDI	67	
B3	VREF1B3	IO	VREF1B3		68	
B3	VREF0B3	IO			69	DQ0R3
B3	VREF0B3	IO			70	DQ0R2
B3	VREF0B3	IO			71	DQ0R1
B3	VREF0B3	IO	DPCLK4		72	DQS0R
B3	VREF0B3	GND				
B3	VREF0B3	VCCIO3				
B3	VREF0B3	IO	VREF0B3		73	
B3	VREF0B3	IO			74	DQ0R0
B3	VREF0B3	IO			75	
B2	VREF0B2	IO			76	DQ1T0
B2	VREF0B2	IO			77	DQ1T1
B2	VREF0B2	IO			78	DQ1T2
B2	VREF0B2	IO			79	DQ1T3
B2	VREF0B2	VCCIO2			80	
B2	VREF0B2	GND			81	
	VREF0B2	VCCINT			82	
	VREF0B2	GND			83	
B2	VREF0B2	IO	DPCLK3		84	DQS0T
B2	VREF0B2	IO	VREF0B2		85	
B2	VREF1B2	IO			86	
B2	VREF1B2	IO			87	
B2	VREF1B2	IO	VREF1B2		88	
B2	VREF1B2	IO			89	
B2	VREF2B2	IO			90	DM1T
B2	VREF2B2	IO	VREF2B2		91	
B2	VREF2B2	IO	DPCLK2		92	DQS1T
	VREF2B2	VCCINT			93	
	VREF2B2	GND			94	
B2	VREF2B2	VCCIO2			95	
B2	VREF2B2	GND			96	
B2	VREF2B2	IO			97	DQ1T4
B2	VREF2B2	IO			98	DQ1T5
B2	VREF2B2	IO		DEV_OE	99	DQ1T6
B2	VREF2B2	IO		DEV_CLRn	100	DQ1T7

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCIO[1..4]	Power	These are I/O supply voltage pins for banks 1 through 4. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, and 3.3-V PCI I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, SSTL2, and SSTL3 I/O standards.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREF[0..2]B[1..4]	I/O, Input	Input reference voltage for banks 1-4. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
VCCA_PLL1	Power	Analog power for PLL1. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL1	Ground	Analog ground for PLL1. The designer can connect this pin to the GND plane on the board.
NC	No Connect	No connect pins should not be connected on the board. They should be left floating.
	Configuration and JTAG Pins	
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input (PS mode), Output (AS mode)	In passive serial configuration mode, DCLK is a clock input used to clock configuration data from an external source into the Cyclone device. In active serial configuration mode, DCLK is a clock output from the Cyclone device (the Cyclone device acts as master in this mode). This is a dedicated pin used for configuration.
DATA0	Input	Dedicated configuration data input pin.
nCE	Input	Active-low chip enable. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
ASDO	I/O, Output	Active serial data output from the Cyclone device. This output pin is utilized during active serial configuration mode. The Cyclone device controls configuration and drives address and control information out on ASDO. In passive serial configuration, this pin is available as a user I/O pin.
nCSO	I/O, Output	Chip select output that enables/disables a serial configuration device. This output is utilized during active serial configuration mode. The Cyclone device controls configuration and enables the serial configuration device by driving nCSO low. In passive serial configuration, this pin is available as a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Dual-purpose pin that can override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the design.
DEV_OE	I/O, Input	Dual-purpose pin that can override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
MSEL[1..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG output pin.
	Clock and PLL Pins	
CLK0	Input	Dedicated global clock input.
CLK2	Input	Dedicated global clock input.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DPCLK[7, 6, 4, 3, 2]	I/O	Dual-purpose clock pins that can connect to the global clock network. These pins can be used for high fan-out control signals, such as clocks, clears, IRDY, TRDY, or DQS signals. These pins are also available as user I/O pins.
Dual-Purpose External Memory Interface Pins		
DQS[0..1][L,R,T,B]	I/O	Optional data strobe signal for use in external memory interfacing. These pins also function as DPCLK pins; therefore, the DQS signals can connect to the global clock network. A programmable delay chain is used to shift the DQS signals by 90 or 72 degrees.
DQ[0..7][L,R,T,B]	I/O	Optional data signal for use in external memory interfacing.
DM[0..1][L,R,T,B]	I/O	Optional data mask output signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die.
2. This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

Bank & PLL Diagram

Version Number	Date	Changes Made
1.5	3/6/2006	Added CRC_ERROR pin in Pin List and Pin Definitions